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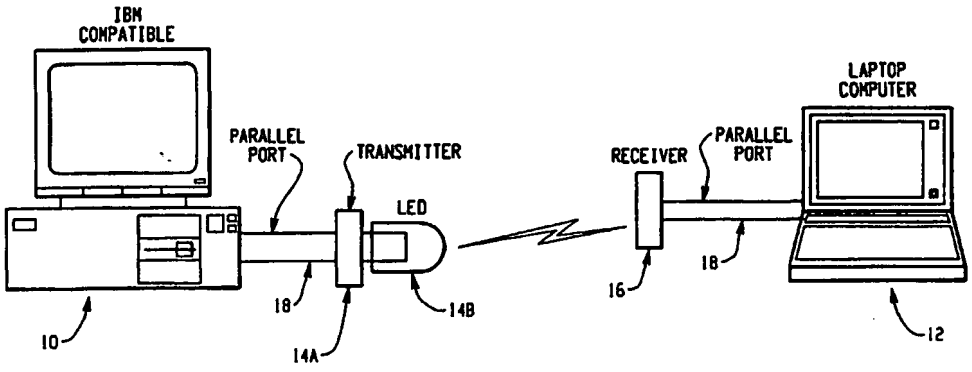

(57) Abstract

A concurrent signaling and data communication system based on the modulation and encoding of digital information using the visible light emitted by light emitting diodes (LEDs) is provided. A general–purpose system includes a transmitter (14a) and receiver circuit (16) coupled to respective computer system (10, 12). The transmitter (14a) is further coupled to an LED beacon (14b), LED dot matrix display (22), or other configuration of LEDs that can be used for simultaneous display and data communication. The computer (10) coupled to the transmitter (14a) is used to control the data communication function of the LEDs, and also may be used to control the display function. A separate computer may also be used to control the display function distinct from the data communication function. The computer (12) coupled to the receiver interprets the data communicated over the optical link between the transmitter (14a) and receiver (16), and may display this information to a user of the system. Two transmitter and receiver designs are provided, one for a non–multi–tasking environment, and the other design for a multi–tasking environment. Several applications of the general–purpose system are provided, including a vehicle speed limiting application, a vehicle location and guidance system application, and a portable traveler information and location system application.

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Concurrent Display and Data Communication using LEDs

RELATED APPLICATIONS

This application claims priority from four provisional applications filed in the United States within one year from the filing date of this application -- United States Serial Nos. 60/078,686; 60/078,684; 60/082,626; and 60/078,691.

FIELD OF THE INVENTION

The present invention relates to the fields of LED display systems and data communications. More specifically, the invention provides a concurrent display and data communication system and methodology using LEDs as the concurrent display and data communication elements. The invention also provides numerous applications of the inventive concurrent display and data communication system.

SUMMARY OF THE INVENTION

The present invention provides a concurrent signaling and data communication system based on the modulation and encoding of digital information using the visible light emitted by one or more light emitting diodes (LEDs). A general-purpose system according to the invention includes transmitter and receiver circuits coupled to respective computer systems. The transmitter is further coupled to an LED beacon, LED dot matrix display, or other configuration of LEDs that can be used for simultaneous display and data communication. The computer coupled to the transmitter is used to control the data communication function of the LEDs, and may also be used to control the display function of the system. A separate computer may alternatively be used to control the display function distinct from the data communication function. The computer coupled to the receiver interprets the data communicated over the optical link between the transmitter and receiver, and may display this information to a user of the system. Two transmitter and receiver designs are provided, one for a non-multi-tasking environment, and the other design for a multi-tasking environment. Several applications of the general-purpose system are also provided, including a vehicle speed limiting application, a vehicle location and guidance system application, and a portable traveler information and location system application.

In addition, the general-purpose system may include one or more executive computer programs operating on the one or more computers coupled to the LED transmitter. These executive computer programs provide software control for the data transmission function of the system, and also provide display control for characters, decorative patterns or messages displayed by the LED beacon or display matrix. The receiver may include a lens system for focusing the light rays from the LEDs onto a photo detector. With appropriate electronics and an executive computer program in the receiving computer, the information in the transmitted light rays from the LEDs is demodulated to provide the transmitted data. The receiver is located at a distance away from the LEDs, and is designed to demodulate the optically transmitted data and then store or display the encoded messages in the associated computer. In order to eliminate flickering in the LEDs caused by the modulated data signals, the frequency at which the LEDs are switched on/off by the transmitted is high enough such that the light emitted by the LEDs appears to be constantly illuminated to the human eye.

According to the teaching of this invention, LEDs can be used as a communication device for the transmission and broadcasting of information and data in addition to their normal function of being an indication or illumination device. Hence, the LED display (or illumination) elements become part of an open-space, wireless optical communication system.

In one respect, the present invention provides a new kind of short-range beacon to support vehicle-to-roadside communications. There are many applications in which this kind of data transfer is advantageous. For example, a traffic light could be constructed with LEDs having a concurrent data transmission function (as well as a display function) as described in this invention. A car driver can then use a receiver to obtain messages from the traffic light. These messages may include location and current traffic information such as street name, speed limit, road conditions, or location of the nearest hospital or gasoline station. Or the driver could check his e-mail through the optical data link. Other applications include file transfers from one computer to another computer, or a portable two-way information transmission and reception system. With such a two-way system, a student could use his/her notebook computer to download his/her assignment questions through an optical data link to the instructor's computer that may be situated at the head of the classroom.

According to one aspect of the invention, a concurrent signaling and data communication system is provided that includes a data display and communication system, a

data receiving system, and one or more LEDs coupled to the data display and communication system, the LEDs emitting a visual display signal and a modulated data communication signal, thereby operating as concurrent elements.

Another aspect of the invention provides a vehicle speed limiting system including a concurrent display and data communication element operating simultaneously as a visual display element and a data communication element, wherein data transmitted by the concurrent display and data communication element is vehicle speed limit data, and an in-vehicle data processing receiver for receiving the transmitted vehicle speed limit data from the concurrent display and data communication element and for processing the received data.

Still another aspect of the invention provides a vehicle location and guidance system. This system includes a concurrent display and data communication element operating simultaneously as a visual display element and a data communication element, wherein data transmitted by the concurrent display and data communication element includes location and guidance information, and an in-vehicle data processing receiver including a central processing unit, a visible light receiver module, and a positioning module for receiving the transmitted location and guidance information from the concurrent display and data communication element and for processing the received data.

Yet another aspect of the invention provides a portable traveler information and location system. This system includes a concurrent display and data communication element operating simultaneously as a visual display element and a data communication element, and a portable traveler information system for receiving data transmitted by the concurrent display and data communication element and for presenting this data to a user of the portable traveler information system.

It should be noted that these are just some of the many aspects of the present invention. Other aspects not specifically listed will become apparent upon reading the detailed description set forth below.

The present invention provides many advantages overly presently known data communication systems. Not all of these advantages are simultaneously required to practice the invention as claimed, and the following list is merely illustrative of the types of benefits that may be provided, alone or in combination. These advantages include: (1) the ability to concurrently operate an LED beacon or other type of display to simultaneously display a pattern of light indicative of some operative condition and to also transmit modulated digital

data; (2) the provision of two types of receiver/transmitter circuits, one for a non-multi-tasking environment, and the other for a multi-tasking environment; (3) the optical link between transmitter and receiver in the present invention is within a portion of the electro-magnetic spectrum that is presently unregulated by the FCC or other similar administrative bodies; (4) short-range operation; (5) low-cost; and (6) ease of deployment.

These are just a few of the many advantages of the present invention, as described in more detail below in terms of the preferred embodiments. As will be appreciated, the invention is capable of other and different embodiments than those specifically set forth below, and its details are capable of modifications in various respects, all without departing from the spirit of the invention. Accordingly, the drawings and description of the preferred embodiments are to be regarded as illustrative in nature and not restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic of a general-purpose concurrent display and data communication system according to the present invention using an LED light beacon as the concurrent element;

FIG. 2 is a schematic of a general-purpose concurrent display and data communication system according to the present invention using an LED dot matrix display as the concurrent element;

FIG. 3 sets forth an exemplary communication protocol of one data frame for use with the present invention;

FIG. 4 is a block diagram of a preferred digital data transmitter for use with the concurrent display and data communication system of the present invention;

FIG. 5 is a block diagram of a preferred digital data receiver for use with the concurrent display and data communication system of the present invention;

FIG. 6 is a block diagram of an alternative digital data transmitter having a memory buffer for use with the concurrent display and data communication system of the present invention;

FIG. 7 is a schematic representation of an operational condition associated with the alternative digital data transmitter in FIG. 6 where the included Serial Input/Output device reading time is slower than a PC coupled to the data transmitter;

FIG. 8 is a schematic representation of an operational condition associated with the alternative digital data transmitter in FIG. 6 where the included Serial Input/Output device reading time is faster than a PC coupled to the data transmitter;

FIG. 9 is a block diagram of an alternative digital data receiver having a memory buffer for use with the concurrent display and data communication system of the present invention;

FIG. 10 is a schematic representation of an operational condition associated with the alternative digital data receiver in FIG. 9 where no idle bytes are received;

FIG. 11 is a schematic representation of an operational condition associated with the alternative digital data receiver in FIG. 9 where idle bytes are received between frames;

FIG. 12 is a timing diagram explaining a source of error in a frame;

FIG. 13 is a diagram of a vehicle speed limiting application of the concurrent display and data communication system of the present invention utilizing LEDs in traffic lights, street lamps, message display board or road beacons;

FIG. 14 is a diagram of a visible light LED transmitter associated with the application shown in FIG. 13;

FIG. 15 is a block diagram of the in-vehicle system associated with the vehicle speed limiting application of FIG. 13;

FIG. 16 is a block diagram of a visible light receiver module associated with the in-vehicle system shown in FIG. 15;

FIG. 17 is a diagram of a vehicle location and guidance system application of the concurrent display and data communication system of the present invention utilizing LEDs in traffic lights, street lamps, message display board or road beacons;

FIG. 18 is a block diagram of the inertial positioning module associated with the system application shown in FIG. 17;

FIG. 19 is a diagram of a portable traveler information system application of the concurrent display and data communication system of the present invention utilizing LEDs in traffic lights, street lamps, message display board or road beacons;

FIG. 20 is a block diagram of a preferred portable traveler information and location unit; and

FIG. 21 is a schematic showing an exemplary user interface for the portable traveler information and location unit shown in FIG. 21.

DETAILED DESCRIPTION OF THE DRAWINGS

1. Concurrent Display and Data Communication System Using LEDs

Turning now to the drawing figures, Figure 1 sets forth a schematic of a general-purpose concurrent display and data communication system according to the present invention using an LED light beacon 14B as the concurrent element. This section of the application describes the general application of the system of the present invention in terms of communication and signaling between two computer systems using an optical channel (or link) operating in a simplex mode (*i.e.* one-way data transfer). Also disclosed in this section are two designs (Design One and Design Two) for a digital data transmitter and a digital data receiver for use with the present invention. These designs are discussed below in connection with Figures 4, 5, 6 and 9. The following issues related to digital communication are also presented: (i) bit error rate; (ii) protocol design; and (iii) coding scheme.

Figure 1 shows data communication and signaling between two computers 10, 12 using an LED light beacon 14B. On the transmitter side, the computer 10 is coupled to the LED light beacon 14B through transmitter circuit 14A via a parallel port 18, typically associated with the computer 10. Embodiments of the transmitter circuit 14A are described in more detail below. In addition, the computer 10 operates an executive computer program, which is used for formatting and controlling the transmission of data over the optical link. One or more LEDs 14B can be used to emit the optical signal, the LEDs 14B operating concurrently as visual signaling devices and as data communication elements (*i.e.* the light emitted by the LEDs 14B functions as a signaling mechanism and as a data communication mechanism). On the receiver side, there are preferably one or more photo-detectors associated with a receiver circuit 16, with an parallel interface circuit 18 to another computer 12, which could be a PC, workstation, notebook computer, or embedded processor. Also coupled to the receiver (although not shown) could be an appropriate lens element for focusing the visible light from the light beacon 14B onto an associated photo-detector(s) or other optical detection element. The data communication signal transmitted from LED transmitter 14B to receiver 16 is preferably formatted as a plurality of data frames, which when received by computer 12, can be unpacked and displayed on the computer.

Figure 2 is a schematic of a general-purpose concurrent display and data communication system according to the present invention using an LED dot matrix display

22 as the concurrent element. This LED display panel 22 is used for providing a visual message signal in the form of light rays for concurrent display of information, as well as data transmission. The transmission side of this system may include two computers 10A, 10B. One of these computers 10A is for controlling the data communication function of the concurrent LED display 22, while the other computer 10B controls the information display function of the LED matrix 22. These computers 10A, 10B are coupled to the LED matrix 22 through an appropriate interface circuit 20, which may include a transmitter circuit (similar to 14A in Figure 1 and those embodiments of 14A discussed below), and may also include circuitry for controlling the display function of the matrix 22. Alternatively, instead of two computers 10A, 10B for controlling the matrix 22, just one computer could manage both functions through the interface circuit 20. An executive computer program runs on both of these computers, one for controlling the data communication function of the display and the other for the visual display control of characters, decorative patterns or messages on the display panel 22.

In general, there are two types of operating system (OS) for IBM-compatible personal computers (PC), such as shown in Figures 1 and 2 : DOS, Windows. The DOS OS is the older type of operating system for the PC. It is characterized by its single task (*i.e.* non-multi-tasking), command-driven environment which was used in all IBM-compatible PCs before Microsoft introduced Windows 3.1 or 95. The first design of the data transmitter and receiver (without memory buffer) shown in Figures 4 and 5 (Design One, below), is the version of the transmitter and receiver for the non-multi-tasking environment. In the Windows 95 environment, the OS has occasional interrupts to all running programs, as it is a multi-tasking environment. These interrupts could disrupt the data transmission process and some data may be lost. There is no such problem in the DOS environment. Hence, the preferred design of the digital data transmitter and receiver shown in Figures 4 and 5 cannot be used in the Windows 95 environment and another version (Design Two), shown in Figures 6 and 9 is provided for the multi-tasking environment. This second design is based on the addition of memory buffers to the interface circuit.

Before turning to a discussion of the two designs for the data transmitter (14 or 22) and receiver (16), it is instructive to consider several data communication aspects of the present invention, including: (i) bit error rate; (ii) protocol design; and (iii) coding scheme.

A. Bit Error Rate (BER)

The inventors have conducted testing of the Bit Error Rate ("BER") of the data general-purpose communication systems described in this application. Factors such as frame size, data rate, lighting environment, distance, and bit pattern of the data frame were varied so that the BERs at different conditions could be characterized. The testing was setup with a direct line-of-sight between the transmitter and the receiver. The factors were varied as follows: (1) Oscillator Frequency: 62.5kbps / 125kbps / 250kbps / 500kbps; (2) Environment: normal / darkness / disturbance; (3) Distance: 2.5 ft / 3 ft; (4) Signal Pattern: 0101... / 0011...; and (5) Frame Size: 1kbyte / 2kbyte / 5kbyte.

A program written in the C++ language was used to facilitate the above-described testing. This program can record the various combinations of conditions including the average error rate, maximum error in a frame and the distribution of errors. A transfer of one megabyte of data was used in each test. All combinations of conditions with bit rate below or equal to 500kbps was used, and the test was repeated many times. This testing established that the BER is so low that it could not be measured with existing experimental setup. Thus, the BER of the present invention is considered very acceptable.

B. Protocol Design

An example communication protocol suitable for data transmission over the optical links shown in Figures 1 and 2 between the transmitter (14 or 22) and receiver (16) is shown in Figure 3. Using this protocol, a stream of digital data to be communicated from transmitter to receiver is converted into a series of data frames 30. Each frame 30 preferably consists of 1024 bytes, although other frame sizes could be utilized. In a preferred frame, there are 48 data blocks 36 with 20 bytes for each data block. Start bytes 34 ("Stx") are added at the beginning of each data block 36. In addition, Synchronization bytes 32 ("Sync") are added at the beginning and near the end of each frame 30, with two idle bytes 38 at the end of the frame.

The number of bytes used for Sync 32 should, in general, be longer than one data block 36 so that even if an 18-byte data block 36 has a pattern exactly equal to the Sync bytes 32, the receiver can still distinguish them. The function of the Stx bytes 34 is to indicate the start of a data block 36, and to allow Sync bytes 32 and data bytes 36 to be distinguished. Operationally, the receiver counts the number of Sync bytes 32. If the number of Sync bytes 32 received is greater than a certain value (for example, greater than 25), which is larger than

the size of the data block 36, then the receiver would know that it is at the start of a frame or the end of a frame. Thirty-two (32) bytes are assigned for the Sync bytes 32 at the beginning of the frame, and 30 bytes at the end so as to give some margin for counting the number of Sync bytes.

The two idle bytes 38 are added at the end to separate frames 30. These idle bytes 38 are also used for synchronizing timing between the transmitter (14 or 22) and the receiver 16. When no data is transmitted, idle bytes 38 are sent out continuously from the transmitter (14 or 22).

At the beginning of a data transmission, the receiver 16 would be receiving the idle bytes 38, which are also for synchronization. When the Sync bytes 32 are received, the receiver 16 would stop the synchronization process and count the Sync bytes 32. If the number of Sync bytes 32 reaches a certain amount (e.g. 25), the receiver would treat the following bytes as data blocks 36. The receiver 16 would then reset a counter and count the number of Sync bytes 32 again. If the count reaches a certain amount (e.g. 25), the receiver 16 would know that it is at the end of a frame 30, and would then use the idle bytes 38 for synchronization of the system again.

It should be noted that although a particular protocol is described in Figure 3, this is just one example of many types of data formatting and framing that could be used with the present invention.

C. Coding Scheme

Human eyes are quite sensitive to variation in light intensity. In the preferred optical link between transmitter and receiver described in this application, the digital data communication process should not affect the light intensity of the LEDs, otherwise the display process of the LEDs will appear to flicker. Therefore, a coding scheme for maintaining constant light intensity during regular data communication is provided. The preferred coding scheme is to use Manchester coding. In Manchester coding, one data bit is mapped into two data bits. For example, data "0" is mapped into "01" with a rising edge, and data "1" is mapped into "10" with a falling edge.

There are three advantages of using Manchester coding. First, it is simple to implement. Second, it can provide an additional clocking signal from the transmitter to the receiver. And third, it can maintain constant brightness for the LEDs with a 50% duty cycle. However, this coding scheme would require two bits to represent one bit of data, and hence

the bandwidth of the system is halved. With Manchester coding, only 512 bytes of actual data can be transmitted by a 1024 byte data frame as described in Figure 3. Although Manchester coding is the preferred coding technique of the invention, it is to be understood that many other coding techniques could also be utilized, and are within the scope of the present invention.

Having described the general-purpose concurrent display and data communication system of the present invention, as well as several issues relating to the design of the optical data communication link, the two designs for the transmitter (14 or 22) and receiver (16) are now presented. Figures 4 and 5 describe the first design, and Figures 6-12 describe the second design. As noted previously, Design One is preferably for use with a PC (or embedded) computer operating the DOS (or other non-multi-tasking operating system), and Design Two is for use with a multi-tasking operating system such as Microsoft Windows. It should be noted that these two designs are merely illustrative of the types of transmitter and receiver circuits that could be used to operate the preferred concurrent display and data communication system. Other designs are possible and are within the scope of the present invention.

Turning back to the drawing figures, Figure 4 is a block diagram of a preferred digital data transmitter 40 for use with the concurrent display and data communication system of the present invention. This design (Design One) is preferably for use with a PC, workstation, or embedded computer operating a non-multi-tasking operating system. Transmitter 40 could be coupled to the beacon LED 14 shown in Figure 1, or the LED dot matrix display 22 shown in Figure 2. This preferred transmitter 40 includes: a parallel port interface 42; a data latch 44; an interface control circuit 43; a system oscillator 56; a system control circuit 50; a baud rate pre-scalar 58; a cycle counter 54; a parallel-to-serial converter 48; and a data transmitter 46.

The parallel port of the PC (10A, 10B or 12) is used for digital data transmission instead of the RS232 port (serial port). This is preferred because the RS232 protocol can vary the brightness of the LEDs and it has a low data rate. The general function of the transmitter 40 is to convert parallel data from the PC into a continuous train of serial data so that it can be transmitted through the optical link between the transmitter and receiver. A protocol and coding scheme similar to that discussed above could also be utilized. In this case, software (an executive program) operating on the computer coupled to the transmitter

40 would include software instructions for formatting the data according to the selected protocol and coding scheme.

The transmitter 40 includes a system oscillator 56 that provides a high frequency signal ("SYSOSC") to a baud rate pre-scalar 58, which is a binary counter for frequency division of the oscillator signal. This circuit 58 provides a programmable system clock frequency ("SYSCLK") for the transmitter 40 and hence the transmission rate can be varied depending on the application and conditions under which the system must operate.

The data latch 44 receives parallel digital data from the parallel port 42 of the PC. It is an octal D-type flip-flop with 3-state outputs. When it receives a clock signal from the PC, parallel data at inputs to the data latch 44 are latched at the outputs (Buffer Data, 8 bit) to the parallel-to-serial converter 48.

The cycle counter 54 and system control 50 circuits are used to govern the timing of transmissions. Coupled to these circuits is a SysINIT signal, which is a system initialization signal from the PC. The cycle counter 54 is a pre-settable synchronous 4-Bit Up/Down counter. It provides a 3-bit counter S[0..2] for decoding of the states by the system control circuit 50 (a 3-to-8 line decoder), which provides a system control function for its operation. When signals S[0..2] from the cycle counter 54 are all zero, the transmitter clock signal TXCLK is low and the data at the inputs of the parallel-to-serial converter 48 are latched.

The GetBuff signal from the system control circuit 50 is connected to the clock signal of the interface control circuit 43, which could be a J-K flip-flop. The falling edge of GetBuff toggles the state of the J-K flip-flop to present a low at BuffCLR to indicate that the transmitter 40 is ready to receive data from the parallel port for transmission.

The parallel-to-serial converter 48, which is an 8-bit parallel-in/serial-out shift register, is used to convert parallel data into serial data and it is controlled by the timing signal TXCLK from the system control circuit 50.

The interface control circuit 43 is also used to produce handshaking signals back to the PC. It is a Dual J-K flip-flop with Reset Negative-Edge Trigger. Its J and K inputs are connected to its own output. When data is not being transmitted, the StrData signal is 0, which clears the flip-flop so that its output is 1. When StrDATA is set to 1 during data transmission, the output of the flip-flop is set to 0. Hence, the function of this flip-flop is to provide the buffer clear signal (BuffCLR) back to the personal computer.

The interface control circuit 43 may also be used to produce an error signal back to the PC. This happens when StrDATA is not set low after the transmission of an 8-bit data byte. In this event, the system error signal (SysERR) is set to 0 and sent to the PC to indicate there is an error of double transmission of the same 8-bit data (duplicated transmission).

After a particular 8-bit data byte has been converted into the appropriate serial data stream by converter 48, this data ("TxData") is then presented to a data transmitter circuit 46, which amplifies these serial signals for coupling to the light source (such as LED beacon of Figure 1, or dot matrix display of Figure 2).

Figure 5 is a block diagram of a preferred digital data receiver 60 for use with the concurrent display and data communication system of the present invention. The receiver module 60 is designed so that digital data can be received using one or more photo-detectors or other type of optical detection device. The receiver 60 receives the transmitted optical signal and converts the received serial data into parallel 8-bit data with appropriate timing. This data can then be transferred to an attached PC via its parallel port. The preferred embodiment of this digital data receiver 60 shown in Figure 5 includes: a parallel port interface 62; a data latch 66; a data receiver 68; a serial to parallel converter 70; an interface control circuit 76; a sync lock circuit 78; a system oscillator 82; a baud rate pre-scalar 80; a cycle count circuit 74, and a system control circuit 72. The operation of these preferred components is described below.

The receiver 60 includes a system oscillator 82 that provides a high frequency signal ("SYSOSC") to a baud rate pre-scalar 80, which is a binary counter for frequency division of the oscillator signal. Using these circuits 80, 82, different system clock frequencies ("SYSCLK") for the receiver 60 can be selected so as to match with the transmission rate of the associated transmitter 40.

The serial-to-parallel circuit 70 is an 8-bit serial-in/parallel-out shift register, which is used to convert serial data into parallel data to the data latch 66. The serial-to-parallel circuit 70 is controlled by the timing signal RXCLK from the system control circuit 72. The data latch 66 is used to latch the parallel digital data for the parallel port 62 of the PC. It is an octal D-type flip-flop with 3-state outputs. When the PC wants to get data, the signal GetDATA from the PC enables the outputs of the data latch 66. Then, as the signal for storing the buffer ("StrBUFF") arrives at the data latch 66, parallel data at its inputs are latched at to its outputs.

The cycle count 74 and system control 72 circuits are used to govern the timing of receiving incoming data at the receiver. The synchronization counter signal SynCNTR from the sync lock circuit 78 is used for the purpose of system synchronization. The cycle count circuit 74 is a pre-settable synchronous 4-Bit Up/Down counter. It provides a 3-bit counter S[0..2] for decoding the states of the system control circuit 72 (a 3-to-8 line decoder), which provides a system control function for its operation.

The system control circuit 72 is a 3-to-8 Line Decoder. It accepts the counter outputs from cycle count circuit 74 S[0..2]. When all the incoming bits S[0..2] are high, the signal StrBUFF is sent to the data latch 66 by the system control circuit 72 so that the data is latched. The data is latched at one-eighth of the master clock frequency so that the shifted data from the serial-to-parallel circuit 70 is latched at an appropriate time. The StrBUFF signal is also sent to the interface control circuit 76, which propagates the data ready signal ("DataRDY") to the PC. If the GetDATA signal cannot be received by the interface control circuit 76, then the system error signal SysERR is sent to the PC instead. This indicates that there is an error in overwriting the incoming 8-bit data.

In order to synchronize the system clock with the received data, the PC sends the SysSYNC signal to the sync lock circuit 78. This halts and resets the count value of the baud rate pre-scalar 80 and cycle count circuit 74 through the SynCNTR signal until the sync lock circuit 78 receives a falling edge of the incoming data through RXDATA. Then, it sends the SysLOCK signal to the PC to indicate that the system has already synchronized with the incoming data.

Having described in detail the preferred design (Design One) for the transmitter and receiver for use with a non-multi-tasking operating system, a second design (Design Two) is now described. This second design is preferably for use with a computer having a multi-tasking operating system. Figures 6-12, below, describe the preferred embodiment of this design.

Figure 6 is a block diagram of a preferred digital data transmitter 110 having a memory buffer for use with the concurrent display and data communication system of the present invention. This design (Design Two) is preferably for use with a computer having a multi-tasking operating system, such as Microsoft Windows. As with the prior design, this transmitter 110 couples to the parallel port 18 of the PC (or laptop or embedded computer) via a parallel port interface 126. The preferred embodiment of this circuit includes: a timing

control circuit 112; a handshaking circuit 114; a first address generator 116 for the transmitter; a serial input/output (SIO) circuit 118; a multiplexer 120, a dual-ported RAM buffer 122; and a second address generator 124 for the PC.

The transmitter is preferably designed so that data is sent through a parallel port 18 in the PC. However, in the Windows 95 environment, there are periodic interrupts to the parallel port during which no data can be delivered. Thus, a transmitter without a memory buffer can suffer serious delays in transmitting data during the period of an interrupt. As a result, a digital data transmitter with a memory buffer is provided so that data can be transmitted through the optical link without interruption.

Another advantage of the configuration shown in Figure 6 is that the transmitter has implemented some required communication protocols in hardware. This can simplify software design and the timing control of the transmitter. The computer can then focus on writing data into the memory buffer.

A dual-port RAM 122 is used as the memory buffer in the transmitter 110. This type of memory is used because a dual-port RAM allows the reading and writing of data at the same time, which simplifies the design. The technique of paging memory management may also be used. The dual-port RAM 122 is divided into two portions called memory pages. When the PC is writing data into one page memory, the transmitter is reading, and sending out data from the other memory page. After completion of writing and reading from a page, the memory pages are swapped, and the transmitter is reading data for transmission from the swapped page that the PC has just written data to. A Serial I/O circuit 118 (SIO) is used to convert parallel data from the PC into a serial data stream for transmission to the receiver.

There are two operational conditions related to timing of data reads and writes that should be considered in implementing the design shown in Figure 6. In the following descriptions, t_{PC} stands for the time it takes for the PC to finish writing one page, and t_{SIO} stands for the time it takes the SIO circuit 118 to finish reading one page. The two conditions are illustrated in Figures 7 and 8, described below.

Figure 7 is a schematic representation of an operational condition associated with the digital data transmitter in Figure 6 where the included Serial Input/Output device reading time is slower than a PC coupled to the data transmitter -- $t_{PC} < t_{SIO}$,that is, SIO reading time is slower than PC writing time. As shown in this figure 90, when the SIO 118 is reading a

data block slower then the PC is writing a data block, the PC just waits for the SIO 118 to complete the reading of data and then swaps memory pages.

Figure 8 is a schematic representation of an operational condition associated with the alternative digital data transmitter where the included Serial Input/Output device reading time is faster than a PC coupled to the data transmitter -- (2) $t_{PC} > t_{SIO}$,that is, SIO reading time is faster than PC writing time. As shown in this figure, 100, when the PC is writing a data block slower than the SIO 118 is reading a data block, the SIO 118 just sends idle bytes (described previously) after the SIO 118 has read and sent the data block. After the PC has completed writing a data block, the memory pages are then swapped for the transmission of another page.

Turning back to Figure 6, a block diagram of the digital data transmitter using a dual-port RAM as a memory buffer is set forth. Coupled to the circuitry shown in Figure 6 is a parallel port interface 126. This interface connects 8-bit data lines, four output control pins and two input control pins to the transmitter circuitry for data transfer and handshaking purposes. The 8-bit data lines represent the byte of data to be transmitted (serially) by the transmitter 110. The four output control pins are named #INIT, #PCStore, FrameStx and PCNext. The two input control pins are named as TerPC and TerSIO.

The #INIT output control pin is used for initializing the transmitter. #PCStore is a signal to indicate the writing of data into the dual-port RAM 122. FrameStx is used to reset the address generator (address counter) for the PC and SIO 124, 116. PCNext is used to increment the address counter for each 8-bit data byte. TerSIO is used to indicate whether the SIO 118 has completed sending out one memory page of data. And TerPC is used to indicate whether the PC has completed writing one memory page of data.

The two address generators 124, 116 for PC and SIO, respectively are preferably counters. They are incremented by signals PCNext and INC (from the timing control circuit 112) to generate addresses for the dual-port RAM 122. They are reset by the FrameStx signal from the PC. They also generate two signals called TerSIO and TerPC to indicate the termination of memory access of the SIO and the PC, respectively.

A handshaking circuit 114 is included for swapping memory pages, also decides when to select idle bytes to be sent out by SIO 118. The handshaking circuit 114 reads two signals, TerSIO and TerPC, from the two address generators, 124, 116, and produces three outputs named PC-MSB , SIO-MSB , and SelSync. PC-MSB is the most significant bit of the address

of the dual-port RAM 122 on the PC side of the memory and SIO-MSB is the most significant bit of the address of the dual-port RAM 122 on the SIO side of the memory. When PC-MSB is set high, SIO-MSB must be set low and vice versa. When the handshaking circuit 114 observes that both TerSIO and TerPC are set, it swaps the states of PC-MSB and PC-SIO so that the memory pages can be swapped. In addition, the handshaking circuit 114 will set the SelSync high when TerPC is set lower then TerSIO. The SelSync signal is used to choose whether idle bytes or the dual-port RAM data is sent by the SIO 118.

The timing control unit 112 is used to generate three signals for the control of timing of the SIO 118. These signals are BitShift, StrBuff and INC. BitShift is a clock signal for the SIO 118 to shift bits to convert parallel data into serial output data. StrBuff is issued per 8-bit period so that the parallel 8-bit data is stored into the buffer on the SIO 118 for transmission. And INC is used to increase the address generator 116 on the SIO side of the dual-port memory 122. The SIO 118 is a shift register to shift bits from the parallel data lines to serial output (TxData Output) to drive the LEDs of the concurrent display and data communication system.

Figure 9 is a block diagram of a digital data receiver having a memory buffer for use with the concurrent display and data communication system of the present invention. This design is for use in combination with the transmitter (with buffer) shown in Figure 6. The preferred receiver 150 design includes: a parallel port interface 168; a synchronization circuit 152; an SIO circuit 154; a latch 156; a dual-port RAM buffer 158; an address generator 160 for the SIO side of the dual-port RAM 158; a handshaking circuit 162; a timing control circuit 164; and an address generator 166 for the PC side of the dual-port RAM 158.

The design of the receiver is similar in many respects to that of the transmitter with memory buffer shown in Figure 6, with the addition of the synchronization circuit 152 and the Sync counter. A dual-port RAM 158 is used as the memory buffer in the receiver, as in the corresponding transmitter circuit. The paging memory management technique discussed above may also be used. According to this technique, the dual-port RAM 158 is divided into two memory pages. When the PC is reading data from one page in memory, the receiver is receiving and writing data to the other page. After completion of the writing and reading from a page, the memory pages are swapped, and the PC then reads data for transmission from the

swapped page that the receiver has just written data to. A Serial I/O (SIO) circuit 154 is used to convert serial data into parallel data, in opposite fashion to the SIO circuit used in the transmitter circuit of Figure 6.

Several operational conditions related to the reception of Idle bytes from the transmitter, as well as a source of error frames should be considered in implementing the design shown in Figure 9. The three conditions are illustrated in Figures 10-12, described below.

Figure 10 is a schematic representation of an operational condition associated with the digital data receiver in FIG. 9 where no idle bytes are received. This situation occurs when, during data transmission, the transmitter does not send out any idle bytes. This can occur when the transmitter's PC is sending data out faster than the transmitter's SIO can transmit the data. The timing requirement for the receiver to receive data in this situation is shown in Figure 10 (130). The receiver's PC would be waiting for another memory page to be filled up by the receiver's SIO 154. After the SIO 154 has received one page, the PC starts to read in data from the page that has just been written by the SIO.

Figure 11 is a schematic representation of an operational condition associated with the digital data receiver in FIG. 9 where idle bytes are received between frames. This occurs when the transmitter's PC is sending out data slower than the transmitter's SIO. The timing requirement for the receiver to receive data in this situation is shown in Figure 11. The receiver PC is waiting for the start of the next incoming frame. After the SIO 154 has received the start of the page, the PC starts to read in data from the page that has just been written by the SIO.

The time for the receiver to receive a frame plus the idle byte should be longer than the time for the PC to read one memory page (i.e. one frame). Otherwise, errors may occur and there would be a possibility of missing a frame. However, the system does not have that error if the time for the PC to write a memory page on the transmitter side is longer than the time for the PC to read a memory page on the receiver side, no matter what the SIO transmission rate is. This idea is explained in Figure 12.

Figure 12 is a timing diagram explaining a source of error in a frame. As shown in this figure, the time for sending idle bytes depends on the time Tpc Tx. If Tpc Tx increases, the time for sending Idle bytes also increases. This means that the time allowed for the receiver PC to read a page also increases. Therefore, as long as Tpc Rx < Tpc Tx, the receiver

can receive all frames without errors. In practice, this can be achieved by adding some delays in the transmitter PC if the receiver PC cannot catch up with the transmission.

Turning back to Figure 9, a block diagram of the digital data receiver using a dual-port RAM as a memory buffer is set forth. Coupled to the circuitry shown in Figure 9 is a parallel port interface 168. This interface 168 includes a byte of 8-bit data lines, three output control pins and three input control pins, which are used for data transfers and handshaking purposes. The four output control pins are named as #INIT, FrameStx and PCNext. The three input control pins are renamed as TerPC, TerSIO and Error.

The #INIT control pin is used for initializing the transmitter. FrameStx is used to reset the address generator 166 (address counter) on the PC side. PCNext is used to increment the address counter for each 8-bit data. TerSIO is used to indicate whether the SIO 154 has completed a receive operation and stored one memory page of data in the dual-port RAM 158. TerPC is used to indicate whether the PC has completed a read operation of one memory page of data. The 8-bit data lines are used for actual data transfers.

The two address generators 166, 160 (for PC and SIO) are counters. They are incremented by signals PCNext and INC to generate addresses for the dual-port RAM 158. They are reset by the FrameStx signal from the PC. They also generate two signals, TerSIO and TerPC, to indicate the termination of memory access for the SIO and PC, respectively.

A handshaking circuit 162 is used to swap memory pages and to produce an error signal (Error) to the PC. It reads two signals, TerSIO and TerPC, and produces three outputs named PC-MSB , SIO-MSB , and Error. PC-MSB is the most significant bit of the address of the dual-port RAM 158 on the PC side and SIO-MSB is the most significant bit of the address of the dual-port RAM 158 on the SIO side. When PC-MSB is set high, SIO-MSB must be set low and vice versa. When the handshaking circuit 162 observes that both TerSIO and TerPC are set high, it swaps the states of PC-MSB and PC-SIO so that the memory page can be swapped. In addition, the handshaking circuit 162 will set the Error signal high when TerPC is set lower then TerSIO. The Error signal is used to alert the PC that a data frame may be lost.

The timing control unit 164 is used to generate three signals for the control of timing of the SIO 154 -- BitShift, StrBuff and INC. BitShift is a clock signal for the SIO 154 to shift bits to convert serial data into parallel input data. StrBuff is issued per 8-bit period so that the

shifted parallel 8-bit data is stored into the latch 156. And INC is used to increase the address generator 160 of the SIO.

A synchronization circuit 152 is added into the receiver. This unit functions to synchronize the timing between the transmitter and the receiver, and to count the number of Sync bytes received. It reads from RxData and the 8-bit parallel data to generate a ValidData signal to the timing control circuit 164. When the circuit has counted enough Sync bytes, ValidData is set so that the frame is available to be written into the dual-port RAM 158.

Having described in detail the general-purpose system of the present invention for concurrent display and data communication using LEDs (including two types of designs for the transmitter and receiver units), it should be understood that the teachings and disclosure of this system can be used in a variety of applications. Three of these numerous applications are described in detail below -- (a) a vehicle speed limiting application, (b) a vehicle location and guidance system application, and (c) a portable traveler information and location system. It should be noted, however, that these are just three of the possible applications of the general system described above. The principles and concepts of the general-purpose concurrent display and data communication system are capable of being applied to numerous other applications not specifically described.

2. Vehicle Speed Limiting Application

Figures 13-16 describe a vehicle speed limiting application using a concurrent display and data communication system having LEDs as the concurrent elements, wherein the LEDs are embedded into traffic lights, street lamps, message display boards, road beacons or the like.

The system shown in Figure 13 may include several components mounted within a vehicle, such as: a visible light receiver module 190, a central processing module 196, a warning or display unit 192, 194, and a vehicle speed sensor 198. The receiver module 190 could operate similarly to the two receiver designs described above for the general-purpose system. Outside of the vehicle, the system may include one or more concurrent sources of display and data communication information using LEDs, such as a street lamp 180, traffic light 182, message display board 184 or a road beacon 186, to name a few. Other types of concurrent display/data communication elements could also be used with this application.

According to the system shown in Figure 13, visible lights emitted by Light Emitting Diodes (LEDs) in traffic lights 182, street lamps 180, message display boards 184 or road

beacons 186 in a prescribed area are modulated so that the visible signal from the LEDs carries a speed limit value. Each of these light sources includes an appropriate transmitter circuit (similar in general principle to those discussed above with respect to the general-purpose system) for modulating the light source with the appropriate data and for energizing the LEDs. In this manner, the LEDs operate concurrently as display elements (such as part of the traffic light 182) and data communication elements (with the speed limit value being the data that is communicated.) Vehicles 188 moving about the prescribed area carry a receiver module 180 for sensing the modulated visible light energy emitted by each traffic light 182, street lamp 180, display board 184 or road beacon 186. The receiver module 190 on the vehicle 188 demodulates and processes the received visible signal to obtain the speed limit information. A processing unit 196 performs the comparison between the vehicle speed from the odometer and the transmitted speed limit information. The in-vehicle system may also provide one or more types of warning and display units 192, 194, which could be augmented by an audio indication, to signal to the driver if his vehicle is exceeding the transmitted speed limit information. Alternatively, some delta-speed could be used so that the warning indicator would only be engaged where the vehicle is exceeding the transmitted speed limit by a predetermined value, such as by 5 miles per hour. In addition, the system could signal the vehicle control unit 210 to decrease the vehicle speed to match the speed limit. In this manner, the system is entirely closed-loop.

Figure 14 is a diagram of a visible light LED transmitter 200 associated with the application shown in Figure 13. This transmitter 200 could be mounted in close proximity to the concurrent display elements 180, 182, 184 or 186, or could be placed at some distance, such as the base of the light pole or in some auxiliary electrical enclosure. This circuit includes a control circuit ("MCU") 202, a plurality of driver circuits 204, and one or more LEDs 206 attached to each driver circuit 204. The appropriate vehicle speed limiting data is packed by the MCU 202 into appropriate data frames according to a particular data protocol. An example coding and protocol scheme is described above with respect to the general-purpose system. This data is then used to drive the LED array 206. The data frames from the MCU 202 may include synchronization bytes that trigger the in-vehicle receiver module 190. Error correction coding techniques may also be used. The driver/buffer circuits 204 provide enough current to drive a set of serially connected LEDs 206, although in the alternative there could be one driver circuit 204 for each LED 206. The driver 204 and LED sets 206 are

repeated to construct the required size of the LED array. It should be noted that the teachings and principles described above with respect to the general-purpose transmitter and receiver designs, as well as the discussion of coding techniques, data communication protocols, etc., could be used with any of the applications described herein.

Figure 15 is a block diagram of the in-vehicle system associated with the vehicle speed limiting application of Figure 13. The in-vehicle system may include a central processing module 196, a visible light receiver module 190, a vehicle speed module 198, a warning unit 192 and a display unit 194. The central processing module 196 preferably controls the other modules. It receives data from the visible light receiver 190 and from the vehicle speed module 198. The purpose of the vehicle speed module 198 is to determine the current speed of the vehicle. The reading may be obtained from sensor data, such as from an odometer. The sensor data is transferred to the central microprocessor 196 through a serial interface. The data from the vehicle speed module 198 and the visible light receiver module 190 is processed by the central processing module 196, and the appropriate information is output to the display 194 and warning 192 units. Also shown is an optional vehicle control unit 210, which can be coupled to the central processing unit 196 in order to automatically adjust the speed of the vehicle to be in compliance with the transmitted speed limit. In this manner, the in-vehicle system operates as a closed-loop remotely actuated governor system that prevents vehicles from exceeding the posted speed limit.

Figure 16 is a block diagram of a visible light receiver module associated with the in-vehicle system shown in Figure 15. It should be noted that the teachings and disclosure of the general-purpose system's two receiver designs could also be utilized in the design shown in Figure 16. As shown, the receiver module 220 may include a light detecting sensor 222 (such as a photodiode, photodiode array, CCD, etc.), a differential amplifier 224, a positive pulse detector 226 and a negative pulse detector 228, and a data recover circuit 230. The light detecting sensor 222 detects the visible light energy and converts it into voltages that are proportional to the received light intensity. The differential amplifier 224 is used to reduce the affects of 50Hz noises induced by fluorescent lights, which may be in the vicinity of the system. It amplifies high-frequency signals such as the change from high to low or from low to high. The output of the differential amplifier 224 includes positive and negative pulses. These pulses are separated by the positive and negative pulse detectors 226, 228 and fed to the data recovery circuit 230. The data recovery circuit 230 includes an SR Flip-Flop that

combines the positive and negative pulses to form a received data stream. The central processing module 196 then extracts the transmitted speed information from this data stream.

3. Vehicle Location and Guidance System Application

FIG. 17 is a diagram of a vehicle location and guidance system application of the concurrent display and data communication system of the present invention utilizing LEDs in traffic lights, street lamps, message display boards, road beacons, or the like. In many respects, this system is similar to the vehicle speed limiting system described above, except that the information transmitted by the concurrent elements 180, 182, 184 or 186 is not vehicle speed information, but instead is information relating to the location of the vehicle and its surrounding geography and traffic conditions.

In this system, a vehicle 188 moving about the prescribed area includes means for sensing 190 the modulated visible light energy emitted by each of a traffic light 182, street lamp 180, display board 184 or road beacon 186. A positioning system 240 (such as dead-reckoning system with digital compass) on the vehicle 188 detects the distance and direction traveled by the vehicle. A receiver 190 on the vehicle 188 demodulates and processes the received signal from the concurrent light sources, and then uses the received location information to calibrate the positioning system 240 in the vehicle 188. The location, guidance and traffic information is shown by displaying means 242 and is also presented as audio signal through a speaker. The displaying means 242 may include a graphical interface for displaying map information, location information, traffic data, the status of a traffic light, and the distance to various services, such as gasoline, hospital or parking, to name but a few.

An example of the in-vehicle visual and audio units 242 is shown in Figure 17. It displays the location of a car on a street map by a crosshair, although other types of indicating means could also be used. On the right side of the display is the information area. In this area, the traffic signal, guidance, location and message information is displayed. For the audio unit, a speaker may output audio information to guide the driver. For example, referring to Figure 17, the car is in the junction of Bonham Road and Pokfulam Road. The traffic light is green. To reach the nearest hospital, the driver has to turn left and drive for 1.5 km. A construction site is nearby and a message display board outputs a message "Road Work" to the driver. The audio unit tells the driver to pass the traffic light and the location of the vehicle.

Figure 18 is a block diagram of the inertial positioning module 240 associated with the system application shown in Figure 17. This module 240 may include an accelerometer

252, gyroscope 250, odometer 254, digital compass 262, A/D converters 260 coupled to the accelerometer 252 and gyroscope 250, controller units 256 and serial interface units 258. The positioning module 240 determines the distance traveled and angle turned by the vehicle 188. The sensor data from the accelerometer 252, gyroscope 250, odometer 254 and digital compass 262 is transferred to the central processing system 196 of the vehicle. The accumulative drift errors exhibited by the inertial sensors are corrected by the positioning information transmitted by the traffic lights, street lamps, message display boards or road beacons.

The positioning module may contain four different kinds of sensors, although not all of these sensors are required, including an odometer 254, accelerometer 252, gyroscope 250, and digital compass 262. The odometer 254 measures the number of turns rolled by the wheels of the vehicle. The distance traveled by the vehicle is then computed by counting the turns represented as electrical pulses. The accelerometer 252 measures the acceleration force experienced by the vehicle. The distance traveled by the vehicle is then computed by integrating the acceleration and then integrating the resultant velocity. The gyroscope 250 measures the angular rate turned by the vehicle. The angle turned by the vehicle is then computed by integrating the measured angular rate. The digital compass 262 is useful for measuring the direction of the vehicle relative to true North. The design of each sensor interface is similar. Each positioning sensor is connected to a controller unit 256 that controls the sensors and performs calculations. The sensor data is then transferred to the central microprocessor 196 through serial interfaces 258

4. Portable Traveler Information and Location System Application

Figure 19 is a diagram of a portable traveler information system application of the concurrent display and data communication system of the present invention. In many respects this system is similar to the systems described above regarding in-vehicle applications, except that in this application the information transmitted by the concurrent elements 180, 182, 184 and 186, is received by a portable unit 290 carried by a pedestrian (or other moving body), which can also transmit information back to the light sources 180, 182, 184, and 186. The concurrent elements may include receiver elements 270 for receiving data transmissions from the portable unit 290. In this manner, a two-way concurrent display and data communication system is provided.

In the system shown in Figure 19, visible lights emitted by Light Emitting Diodes (LEDs) in traffic lights 182, street lamps 180, message display boards 184 or road beacons 186 (or the like) in a prescribed area are modulated so that the visible signal carries a location, local area map, public transportation stations, major sites/buildings in the neighborhood area and/or guidance information or other types of information or data. The traffic lights 182, street lamps 180, message display boards 184 or road beacons 186 may also include means for receiving 270 a traveler's request signal. Traveler or pedestrian carries a portable information and location system 290, which includes means for receiving modulated information from the concurrent display/data communication elements (180, 182, 184, 186) and for transmitting information back to receivers 270 associated with these elements. The location, travel and guidance information can be shown by displaying means 272 that is part of the portable system 290, and can also be presented as audio signals through an included speaker 280. The displaying means 272 may include a map display 278 with cross-hairs to indicate the position of the traveler, an information interface 274 for displaying a menu of information selections to the traveler, a location interface 276 for displaying a menu of location selections to the traveler, a selection button 282, and scroll buttons 284 for moving through the interface menus. Other elements may also be provided in the interface.

Figure 20 is a block diagram of a preferred portable traveler information and location unit 290. This unit 290 may include a visible light receiver module 298, a transmitter module 292, a central processing module 294, a visual and audio unit 272, 280, and a user input module 296. The receiver module 298 receives the modulated visible light energy from the concurrent display/data communication elements and demodulates it to obtain the information. The information is then processed by the central processing module 294, which determines what information to display or present, and how to display it. The central processing module 294 contains a microprocessor system that controls the other modules and also performs data transfer. The traveler commands the portable module 290 using the user input module 296. The user input module may provide manual input, such as a selection button 282 or scroll keys 284, or could, in the alternative, provide a speech recognition module so that the traveler can command the unit using voice commands. Other types of input means are also possible.

Input commands are transferred from the central processing module 294 to the transmitter module 292. The transmitter module 292 sends the user request signal to the

receiver units 270 associated with the traffic lights 182, street lamps 180, message display boards 184 or road beacons 186. In this manner, an interactive travel and guidance system is provided in which the traveler can choose what information to download from the concurrent display/data communication system.

An example of the operation of the portable traveler information system is shown in Figure 19. On the user interface 272, the location of the traveler or pedestrian is displayed on a local street map with a cross. The local street map is downloaded from the concurrent elements (180, 182, 184, 186). These elements may be connected by a network 286 to other elements and/or computer systems that provide the traveler with the requested information.

On the right side of the user interface is the information selection area 274 and the location information area 276. In these areas, the traveler can select what information to be downloaded from the concurrent elements. In the example, if 'Restaurant' is selected, then the corresponding information regarding nearby restaurants is downloaded. The location of these nearby restaurants is then displayed on the map and some introduction of the restaurants may also be provided in the pop up menu in the information area. Other information that can be transmitted may include hospital, police station, shopping mall, commercial building, airline office, taxi station, MTR station, or airport bus stop information, to name a few. The traveler can also enter their destination into the portable module 290 before embarking on a trip. The position of the destination will be displayed on the local map if the destination falls on it. Also, best routes can be calculated and displayed on the map. Voice signals may be given by the system if the traveler is nearby the destination.

Figure 21 is a schematic showing an exemplary user interface for the portable traveler information and location unit 290 shown in Figure 20. In the information area 274, a user can select what information he wants to review, such as "Hospital", "Police Station", "Restaurant", etc. For example, suppose the traveler wants to find a restaurant for a dinner. He can approach a nearby traffic light, street lamp, message display board or road beacon that is coupled to the system. Then, he can select 'Restaurant' in the information menu. A pop-up menu 274A will be displayed in the information area. From this, he can choose the kind of restaurant he wants, such as a Chinese restaurant. Another pop-up menu 274B will then appear. From this, he can select the class of restaurants he can afford. Then, a list 274C of nearby restaurants that suit his needs is displayed. Finally, he can see the information of the restaurants in the list 274D. In the same manner, each of the information selections may

include a series of additional pop-up menus in the information area for further refining the traveler's search for relevant information.

The preferred embodiments and several applications of the inventive system described above are presented only by way of example and are not meant to limit the scope of the present invention, which is defined by the claims. Other elements and steps could be used in place of those shown. In addition, many other applications of the general-purpose concurrent display and data communication system are also possible and are within the scope of the present invention.

What is claimed:

1. A concurrent signaling and data communication system, comprising:

a data display and communication system;

a data receiving system; and

one or more LEDs coupled to the data display and communication system, the LEDs emitting a visual display signal and a modulated data communication signal.

2. The system of claim 1, wherein the data display and communication system comprises:

a first computer;

a data transmitter circuit coupled to the first computer and the one or more LEDs; and

a data communication computer program operating on the first computer for generating a digital data signal.

3. The system of claim 2, wherein the data display and communication system further comprises a data display computer program operating on the first computer for controlling the generation of the visual display signal.

4. The system of claim 2, wherein the data display and communication system further comprises:

a second computer; and

a data display computer program operating on the second computer for controlling the generation of the visual display signal.

5. The system of claim 1, wherein the data receiving system receives the modulated data communication signal emitted by the one or more LEDs.

6. The system of claim 5, wherein the data receiving system includes:

a optical sensing element;

a data receiver circuit coupled to the optical sensing element; and

a receiving computer system coupled to the data receiving circuit.

7. The system of claim 6, further including a lens for receiving the modulated data communication signal from the one or more LEDs and for focusing the modulate data communication signal on the optical sensing element.

8. The system of claim 6, wherein the optical sensing element is a photodetector.

9. The system of claim 1, wherein the one or more LEDs are configured as a two-dimensional dot-matrix display.

10. The system of claim 6, further including a data communication computer program operating on the receiving computer system for controlling the reception of the modulated data communication signal.

11. The system of claim 2, wherein the data transmitter circuit is coupled to the first computer via a parallel interface.

12. The system of claim 9, wherein the dot-matrix display can generate visual display signals including characters, words, pictures, graphics or decorative patterns.

13. The system of claim 2, wherein the data transmitter circuit includes modulation circuitry for generating the modulated digital data signal from the digital data signal generated by the data communication computer program operating on the first computer.

14. The system of claim 13, wherein the data transmitter circuit applies the modulated digital data signal to the one or more LEDs.

15. The system of claim 14, wherein the modulated digital data signal emitted by the LEDs is at a high frequency so that the LEDs appear constantly illuminated to a human eye.

16. The system of claim 6, wherein the data receiving circuit includes means for demodulating the modulated digital data signal.

17. The system of claim 2, wherein the first computer operates a non-multi-tasking operating system.

18. The system of claim 2, wherein the first computer operates a multi-tasking operating system.

19. The system of claim 1, wherein the modulated digital data signal is formatted into a plurality of data frames.

20 The system of claim 20, wherein each data frame includes:

beginning frame synchronization bytes;

a plurality of start bytes and data bytes; and

ending frame synchronization bytes.

21. The system of claim 21, wherein each data from further includes idle bytes.

22. The system of claim 1, wherein the modulated digital data signal is encoded using manchester coding.

23. The system of claim 2, wherein the data transmitter circuit includes:

a parallel port interface for receiving the digital data signal from the first computer;

a parallel-to-serial converter for converting the digital data signal to a serial data stream; and

modulation control circuitry coupled to the parallel-to-serial converter for controlling the clock rate of the converter in order to generate the modulated digital data signal.

24. The system of claim 23, wherein the modulation control circuitry includes:

a system oscillator; and

a baud-rate pre-scalar coupled to the system oscillator for generating a selectable modulation frequency for clocking the parallel-to-serial converter.

25. The system of claim 23, wherein the data transmitter circuit further includes a data latch coupled between the parallel port and the parallel-to-serial converter.

26. The system of claim 6, wherein the data receiver circuit includes:

a serial-to-parallel converter for converting the modulated digital data signal to a serial data stream;

demodulation control circuitry coupled to the serial-to-parallel converter for controlling the clock rate of the converter in order to recover the digital data signal; and

a parallel port interface for coupling the recovered digital data signal to the receiving computer system.

27. The system of claim 26, wherein the demodulation control circuitry includes:

a system oscillator; and

a baud-rate pre-scalar coupled to the system oscillator for generating a selectable demodulation frequency for clocking the serial-to-parallel converter.

28. The system of claim 26, wherein the data receiver circuit further includes a data latch coupled between the parallel port and the serial-to-parallel converter.

29. The system of claim 27, wherein the data receiver circuit further includes a clock synchronization circuit for ensuring that the demodulation frequency matches the modulation frequency of the received modulated digital data signal.

30. The system of claim 2, wherein the data transmitter circuit includes:

a parallel port interface for receiving the digital data signal from the first computer;

a serial input/output (SIO) circuit for converting the parallel digital data signal into a serially modulated digital data signal; and

a memory buffer coupled between the parallel port interface and the SIO circuit.

31. The system of claim 30, wherein the memory buffer is a dual-port RAM.

32. The system of claim 31, wherein the data transmitter circuit further includes a pair of address generators for each port of the dual-port RAM.

33. The system of claim 30, wherein the data transmitter circuit further includes a timing control circuit for controlling the modulation frequency of the SIO circuit.

34. The system of claim 6, wherein the data receiver circuit includes:

a serial input/output (SIO) circuit for converting the received modulated digital data signal into a demodulated parallel digital data signal.

a parallel port interface for coupling the demodulated digital data signal to the receiving computer system; and

a memory buffer coupled between the parallel port interface and the SIO circuit

35. The system of claim 34, wherein the memory buffer is a dual-port RAM.

36. The system of claim 35, wherein the data receiver circuit further includes a pair of address generators for each port of the dual-port RAM.

37. The system of claim 34, wherein the data receiver circuit further includes a timing control circuit for controlling the demodulation frequency of the SIO circuit.

38. A vehicle speed limiting system, comprising:

a concurrent display and data communication element operating simultaneously as a visual display element and a data communication element, wherein data transmitted by the concurrent display and data communication element is vehicle speed limit data; and

an in-vehicle data processing receiver for receiving the transmitted vehicle speed limit data from the concurrent display and data communication element and for processing the received data.

39. The system of claim 38, wherein the concurrent display and data communication element is a street lamp, traffic light, message display board or road beacon.

40. The system of claim 38, wherein the concurrent display and data communication element includes one or more LEDs.

41. The system of claim 40, wherein the LEDs emit a modulated digital signal that carries the vehicle speed limit data.

42. The system of claim 38, wherein the in-vehicle data processing receiver includes:

a visible light receiver module for receiving the vehicle speed limit data transmitted by the concurrent display and data communication element; and

a central processing module coupled to the visible light receiver module for processing the vehicle speed limit data.

43. The system of claim 42, wherein the vehicle speed limit data comprises a modulated digital data signal, and wherein the visible light receiver module includes means for demodulating the modulated digital data signal to recover the vehicle speed limit data.

44. The system of claim 42, wherein the in-vehicle data processing receiver further includes a vehicle speed module for providing the current speed of the vehicle.

45. The system of claim 44, wherein the central processing module compares the transmitted vehicle speed limit data with the current speed of the vehicle and generates a warning signal if the current speed of the vehicle is greater than the transmitted vehicle speed limit data.

46. The system of claim 45, wherein the in-vehicle data processing receiver further includes a warning unit or a display unit coupled to the warning signal generated by the central processing module for alerting the driver of the vehicle that the current speed of the vehicle exceeds the transmitted speed limit data.

47. The system of claim 45, wherein the in-vehicle data processing receiver further includes a vehicle control unit for automatically adjusting the speed of the vehicle if the current speed of the vehicle exceeds the transmitted speed limit data.

48. The system of claim 42, wherein the visible light receiver module includes:

a light detecting sensor; and

a data recovery circuit coupled to the sensor for demodulating the signal received by the light detecting sensor.

49. The system of claim 48, wherein the visible light receiver module further includes a differential amplifier and a positive and negative pulse detector coupled between the light detecting sensor and the data recovery circuit.

50. A vehicle location and guidance system, comprising:

a concurrent display and data communication element operating simultaneously as a visual display element and a data communication element, wherein data transmitted by the concurrent display and data communication element includes location and guidance information; and

an in-vehicle data processing receiver including a central processing unit, a visible light receiver module, and a positioning module for receiving the transmitted location and guidance information from the concurrent display and data communication element and for processing the received data.

51. The system of claim 50, wherein the location and guidance information includes positioning information, traffic information, map information, road work conditions, traffic signal status, or directions to nearby facilities.

52. The system of claim 50, wherein the in-vehicle data processing receiver further includes a visual and audio display unit for displaying the information transmitted by the concurrent display and data communication element.

53. The system of claim 52, wherein the visual and audio display unit provides a local street map showing the current position of the vehicle.

54. The system of claim 52, wherein the visual and audio display unit provides a speaker for providing audio directions to the driver.

55. The system of claim 52, wherein the visual and audio display unit provides a display of the current status of a nearby traffic light.

56. The system of claim 52, wherein the visual and audio display unit provides a display of directions to nearby facilities.

57. The system of claim 50, wherein the central processing unit receives the location and positioning information transmitted by the concurrent display and data communication element and uses this information to calibrate the positioning module.

58. The system of claim 50, wherein the positioning module includes one or more inertial sensors, such as an accelerometer, a gyroscope, an odometer or a digital compass.

59. The system of claim 50, wherein the positioning module includes an accelerometer, an analog to digital converter, a controller and a serial interface to the central processing module.

60. The system of claim 58, wherein the inertial sensors drift overtime, and wherein this drift is corrected by the central processing module based on the location and guidance information transmitted by the concurrent display and data communication element.

61. A portable traveler information and location system, comprising:

a concurrent display and data communication element operating simultaneously as a visual display element and a data communication element; and

a portable traveler information system for receiving data transmitted by the concurrent display and data communication element and for presenting this data to a user of the portable traveler information system.

62. The system of claim 61, wherein the concurrent display and data communication element includes a receiver for receiving information transmitted by the portable traveler information system.

63. The system of claim 61, further comprising a plurality of concurrent display and data communication elements coupled together by a network.

64. The system of claim 61, wherein the concurrent display and data communication element includes one or more LEDs for emitting a modulated digital data signal.

65. The system of claim 64, wherein the portable traveler information system includes a receiver for receiving the modulated digital data signal and means for demodulating the modulated signal to recover the digital data signal.

66. The system of claim 61, wherein the portable traveler information system includes:

a visible light receiver module;

a central processing unit;

a user-input module;

a display unit;

an audio unit; and

a transmitter module.

67. The system of claim 61, wherein the portable traveler information system includes a graphical user interface for displaying information to the user of the system.

68. The system of claim 66, wherein the display unit provides a graphical display of information received from the concurrent display and data communication element by the visible light receiver module.

69. The system of claim 67, wherein the graphical user interface includes a map showing the current location of the user of the system.

70. The system of claim 67, wherein the graphical user interface includes a plurality of pop-up menus that describe facilities nearby the current location of the user of the system.

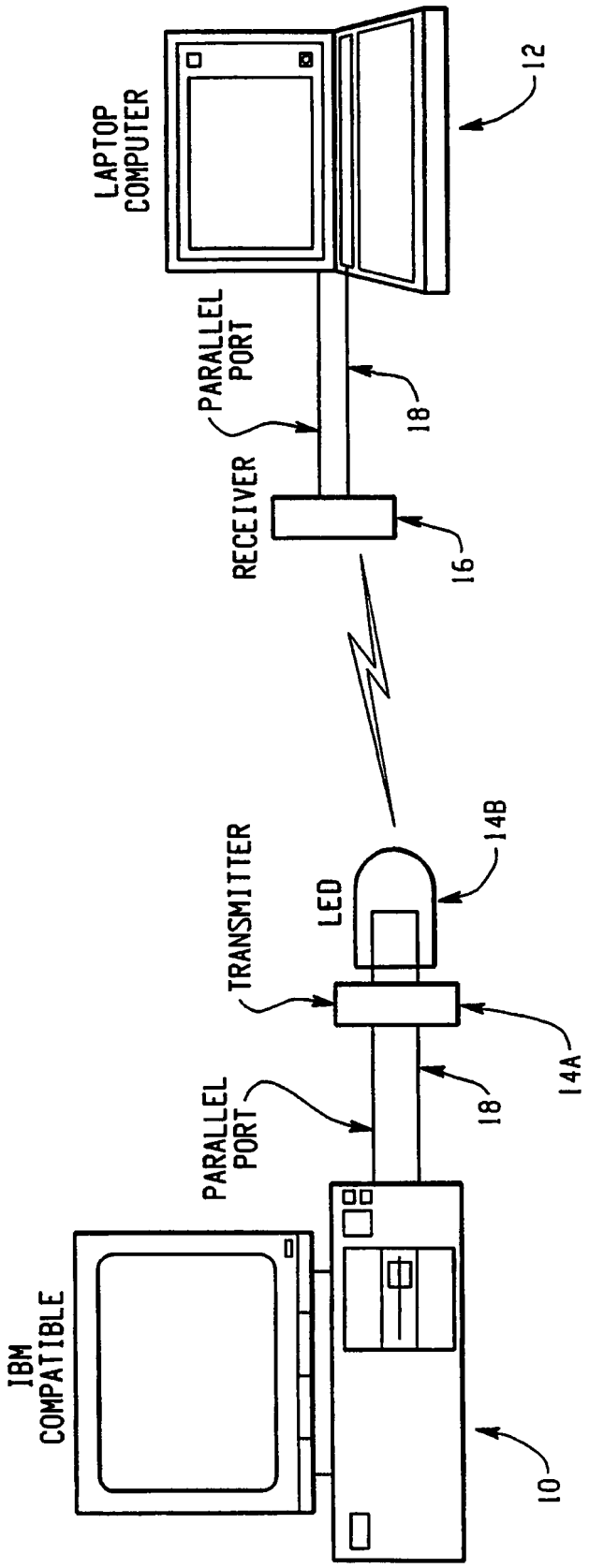

LAPTOP COMPUTER
12
PARALLEL PORT
18
RECEIVER
16
TRANSMITTER
LED
14B
14A
PARALLEL PORT
18
IBM COMPATIBLE
10

Fig. 1

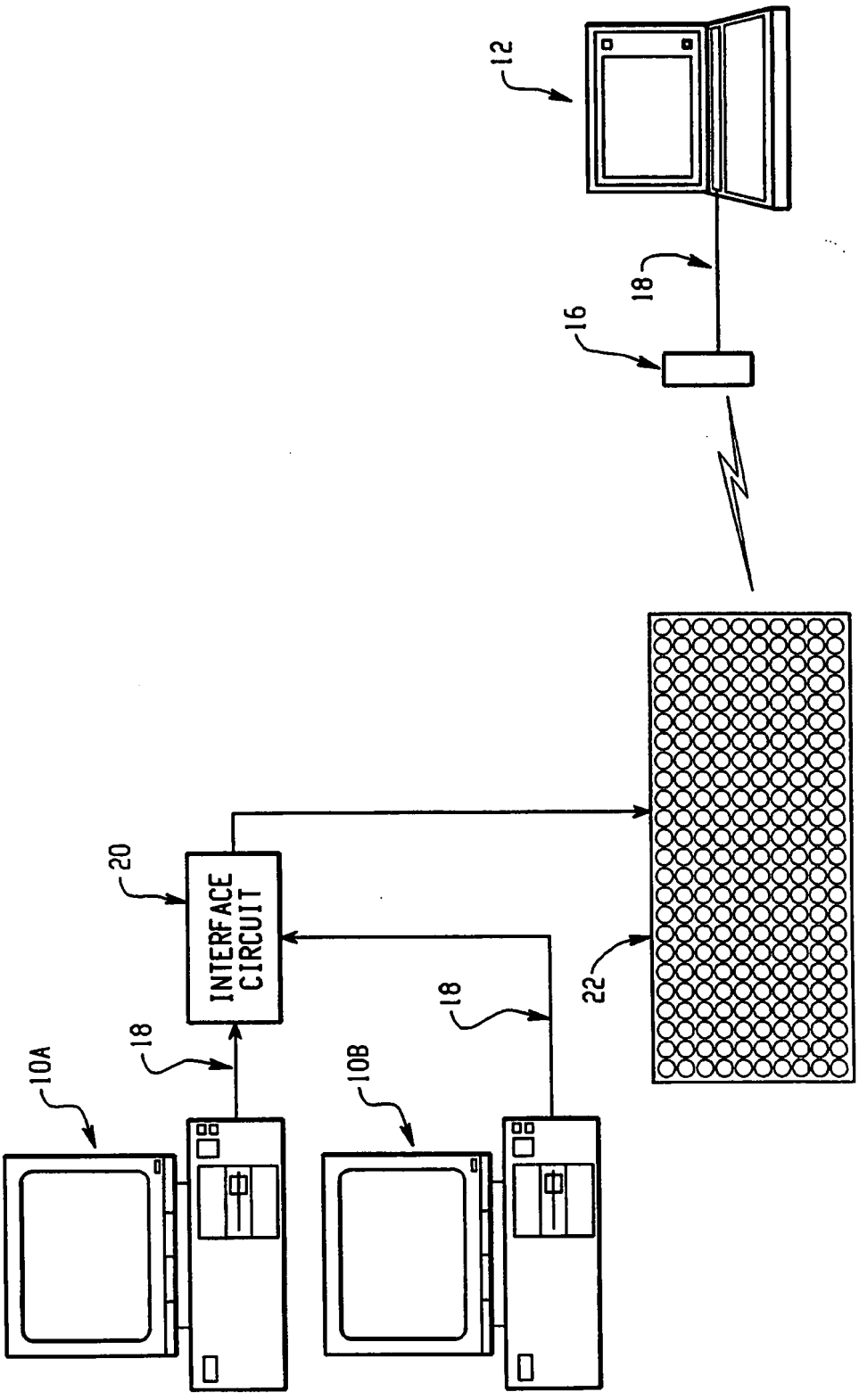


Fig. 2

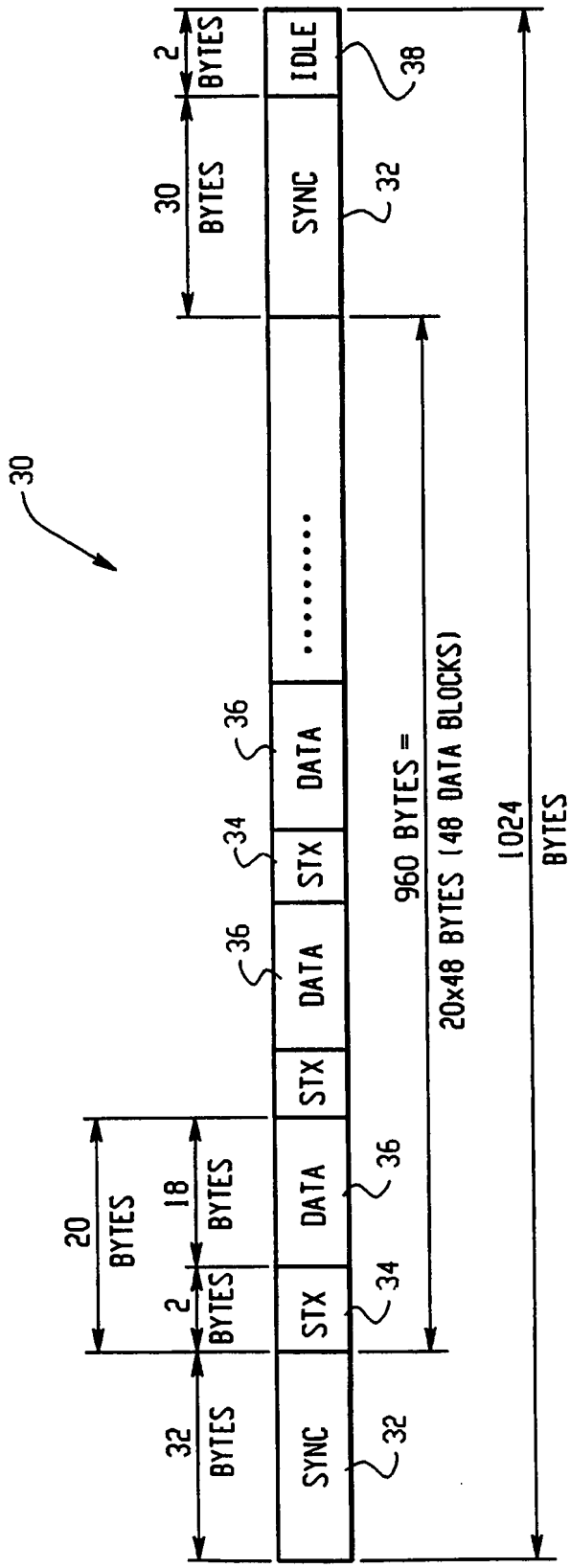

30
2 BYTES
IDLE
38
30 BYTES
SYNC
32
.....
36
DATA
34
STX
36
DATA
STX
960 BYTES =
20x48 BYTES (48 DATA BLOCKS)
1024 BYTES
20 BYTES
18 BYTES
36
DATA
2 BYTES
STX
34
32 BYTES
SYNC
32

Fig. 3

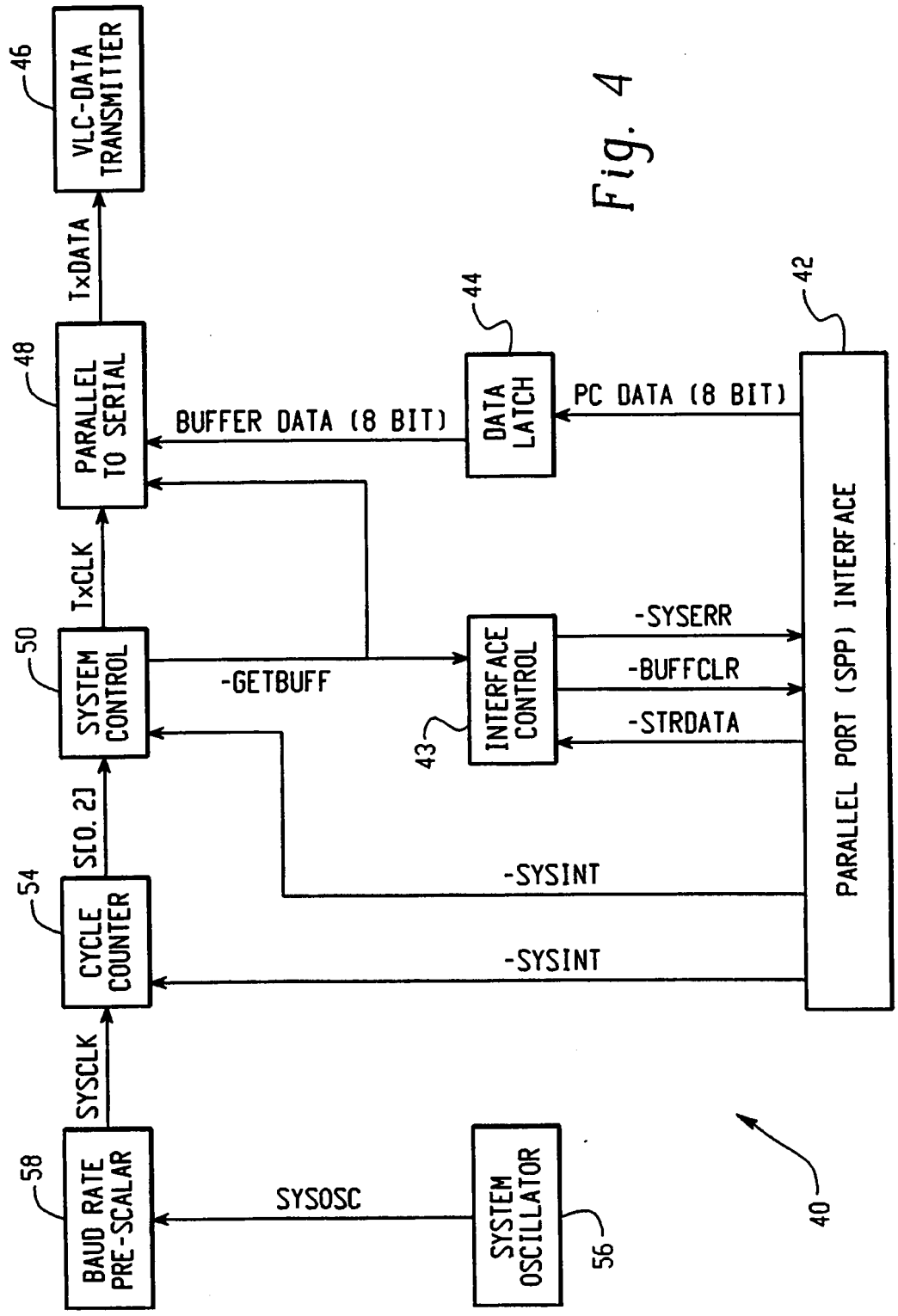

VLC-DATA TRANSMITTER
46
TxDATA
PARALLEL TO SERIAL
48
BUFFER DATA (8 BIT)
DATA LATCH
44
PC DATA (8 BIT)
42
TxCLK
SYSTEM CONTROL
50
-GETBUFF
INTERFACE CONTROL
43
-SYSERR
-BUFFCLR
-STRDATA
PARALLEL PORT (SPP) INTERFACE
SI0.2J
CYCLE COUNTER
54
-SYSINT
-SYSINT
SYSCLK
BAUD RATE PRE-SCALAR
58
SYSOSC
SYSTEM OSCILLATOR
56
40

Fig. 4

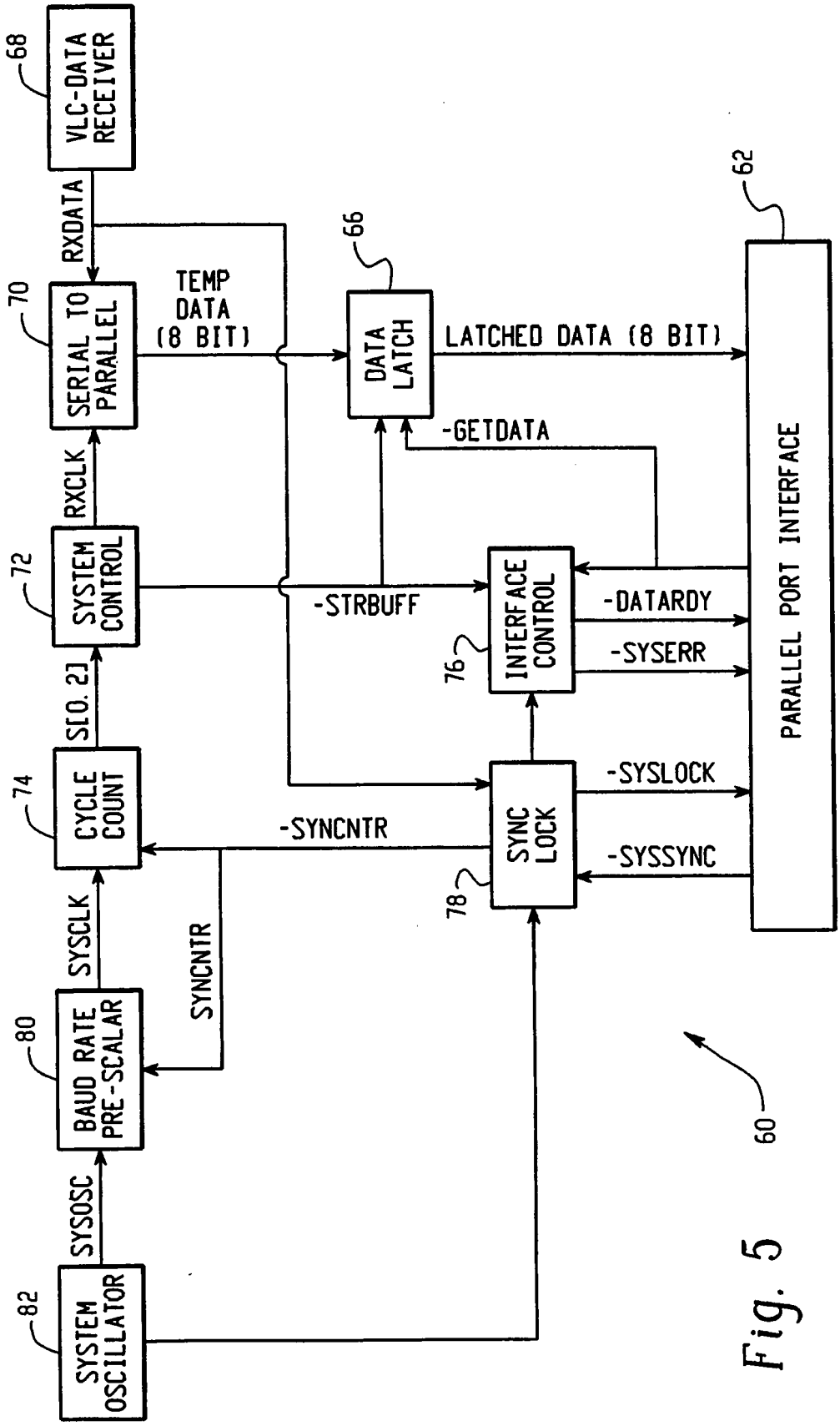

68
VLC-DATA RECEIVER
RXDATA
70
SERIAL TO PARALLEL
TEMP DATA (8 BIT)
66
DATA LATCH
LATCHED DATA (8 BIT)
62
PARALLEL PORT INTERFACE
-GETDATA
RXCLK
72
SYSTEM CONTROL
-STRBUFF
INTERFACE CONTROL
76
-DATARDY
-SYSERR
SIO. 2]
74
CYCLE COUNT
-SYNCNTR
SYNC LOCK
78
-SYSLOCK
-SYSSYNC
SYSCLK
SYNCNTR
80
BAUD RATE PRE-SCALAR
SYSOSC
82
SYSTEM OSCILLATOR
60

Fig. 5

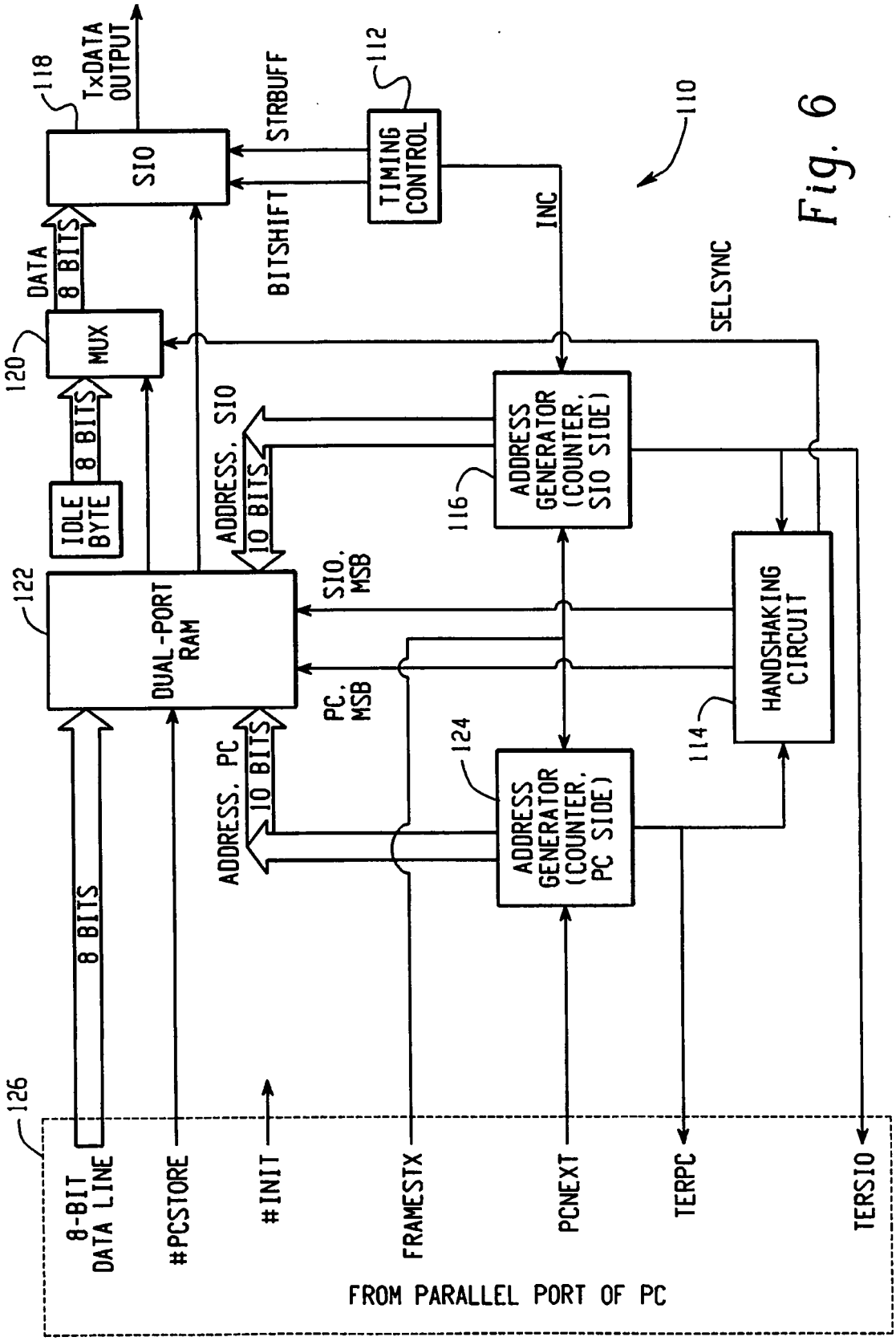

118
TxDATA OUTPUT
SIO
STRBUFF
112
TIMING CONTROL
110
DATA
8 BITS
BITSHIFT
INC
SELSYNC
120
MUX
8 BITS
IDLE BYTE
ADDRESS, SIO
10 BITS
116
ADDRESS GENERATOR (COUNTER, SIO SIDE)
122
DUAL-PORT RAM
SIO, MSB
PC, MSB
HANDSHAKING CIRCUIT
114
124
ADDRESS, PC
10 BITS
ADDRESS GENERATOR (COUNTER, PC SIDE)
8 BITS
126
8-BIT DATA LINE
#PCSTORE
#INIT
FRAMESTX
PCNEXT
TERPC
TERSIO
FROM PARALLEL PORT OF PC

Fig. 6

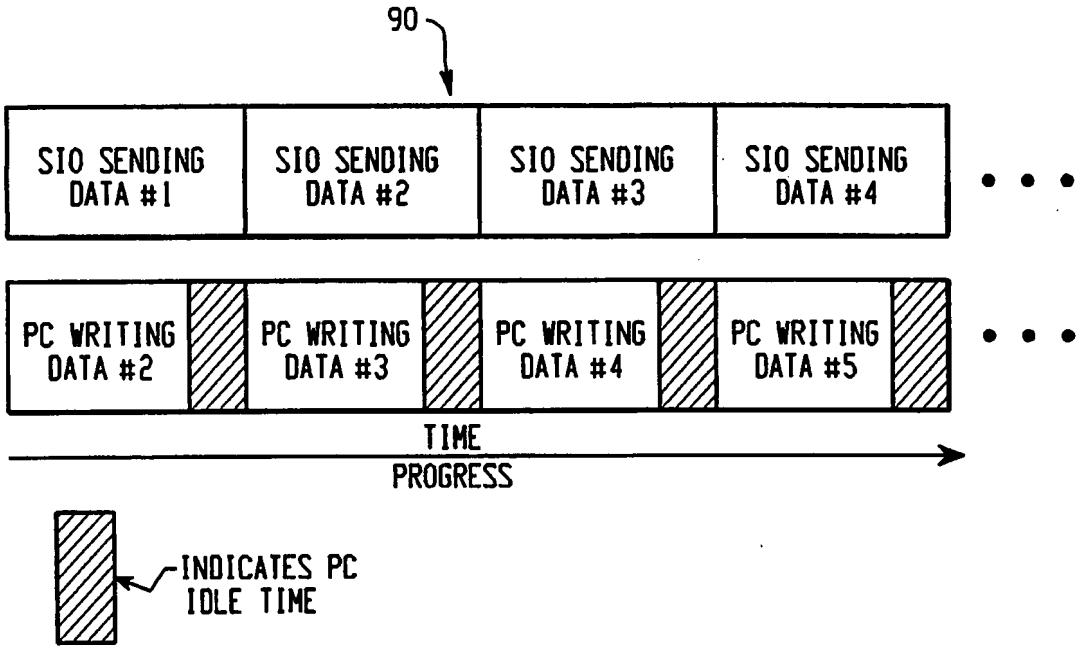

90
SIO SENDING DATA #1
SIO SENDING DATA #2
SIO SENDING DATA #3
SIO SENDING DATA #4
PC WRITING DATA #2
PC WRITING DATA #3
PC WRITING DATA #4
PC WRITING DATA #5
TIME PROGRESS
INDICATES PC IDLE TIME

Fig. 7

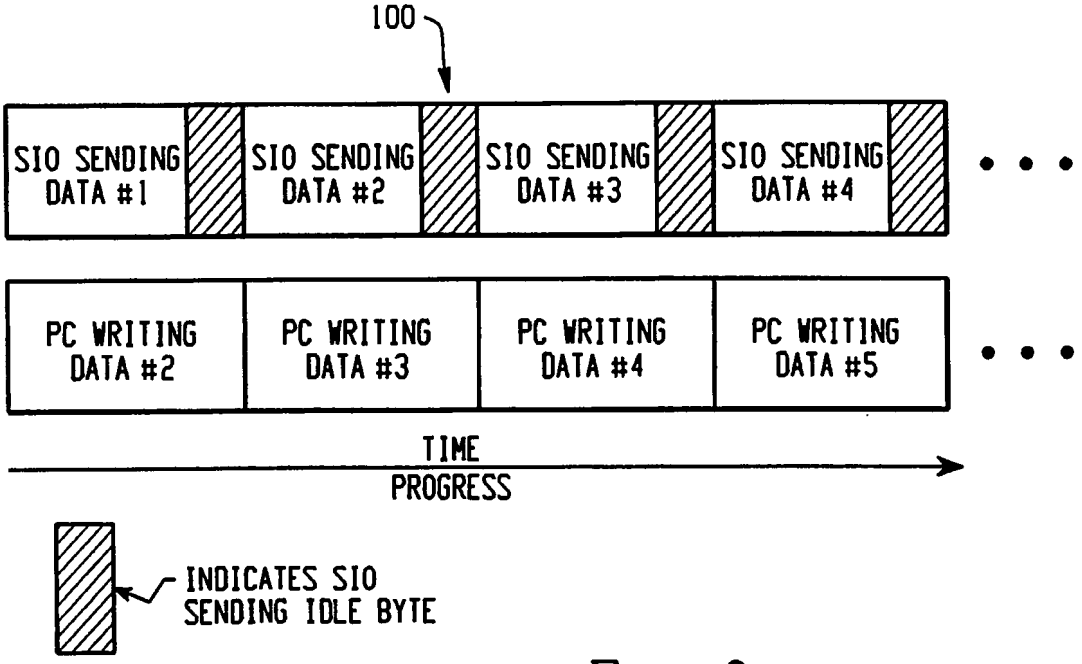

100
SIO SENDING DATA #1
SIO SENDING DATA #2
SIO SENDING DATA #3
SIO SENDING DATA #4
PC WRITING DATA #2
PC WRITING DATA #3
PC WRITING DATA #4
PC WRITING DATA #5
TIME PROGRESS
INDICATES SIO SENDING IDLE BYTE

Fig. 8

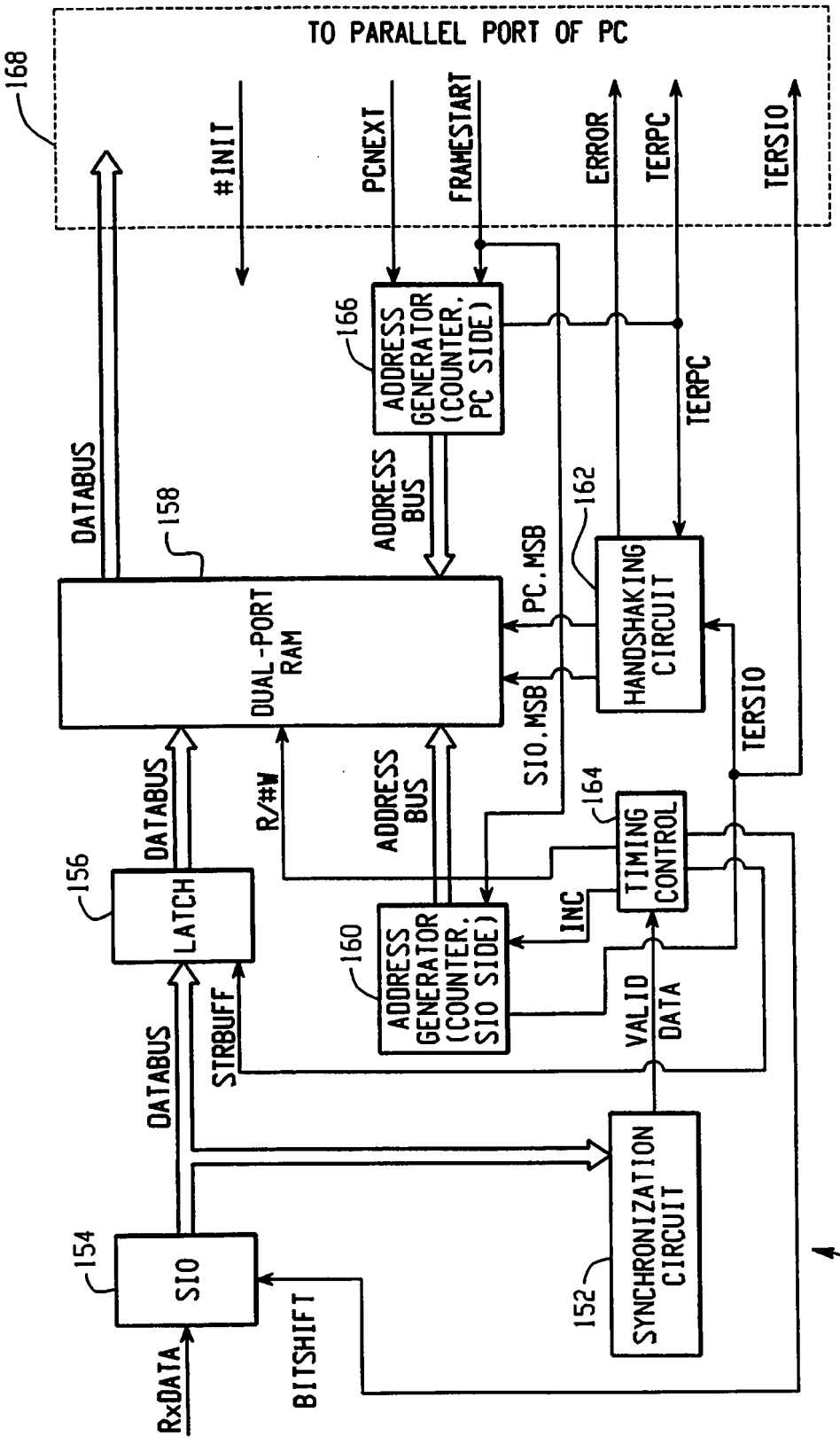

TO PARALLEL PORT OF PC
168
#INIT
PCNEXT
FRAMESTART
ERROR
TERPC
TERSIO
166
ADDRESS GENERATOR (COUNTER, PC SIDE)
ADDRESS BUS
DATABUS
158
DUAL-PORT RAM
PC.MSB
162
HANDSHAKING CIRCUIT
SIO.MSB
TERSIO
R/#W
ADDRESS BUS
164
TIMING CONTROL
DATABUS
156
LATCH
160
ADDRESS GENERATOR (COUNTER, SIO SIDE)
INC
VALID DATA
STRBUFF
DATABUS
154
SIO
RxDATA
BITSHIFT
152
SYNCHRONIZATION CIRCUIT
150

Fig. 9

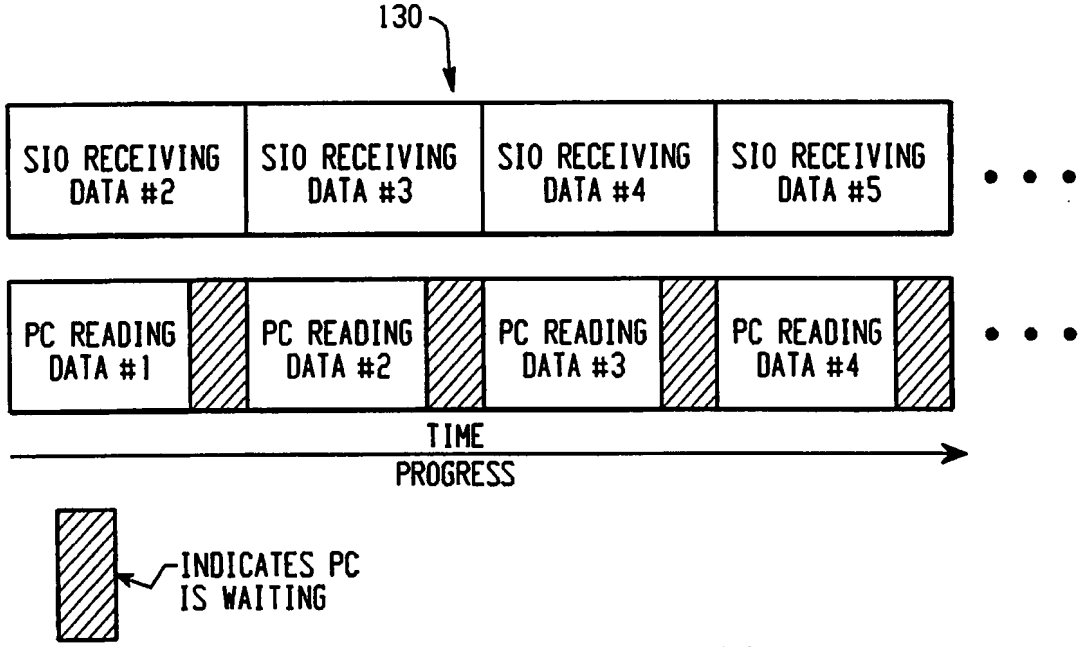

130
SIO RECEIVING DATA #2
SIO RECEIVING DATA #3
SIO RECEIVING DATA #4
SIO RECEIVING DATA #5
PC READING DATA #1
PC READING DATA #2
PC READING DATA #3
PC READING DATA #4
TIME PROGRESS
INDICATES PC IS WAITING

Fig. 10

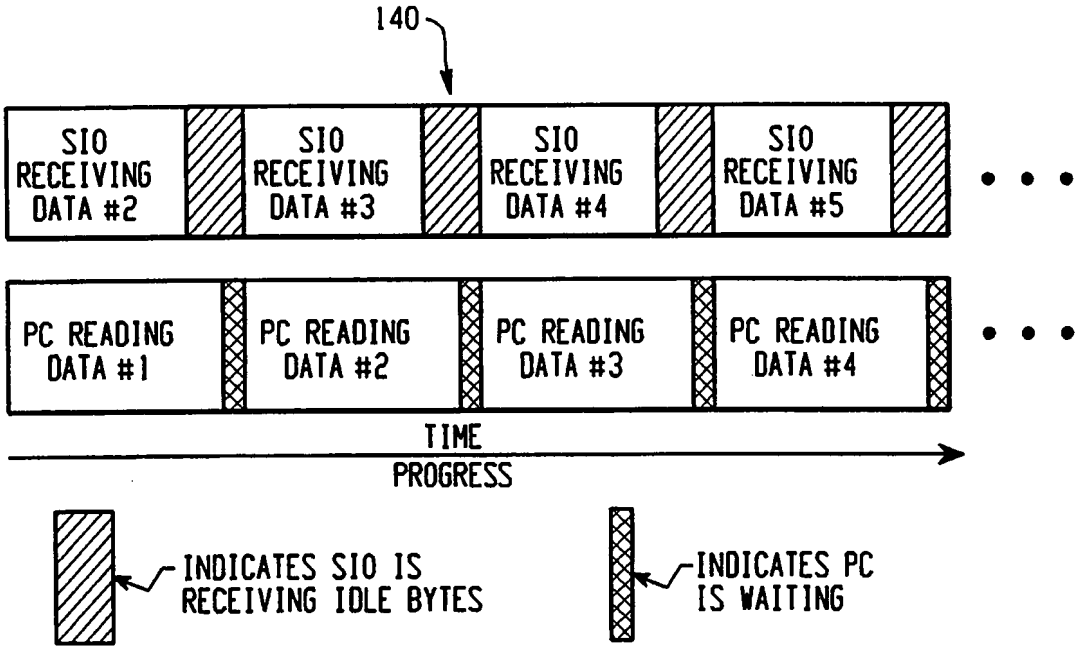

140
SIO RECEIVING DATA #2
SIO RECEIVING DATA #3
SIO RECEIVING DATA #4
SIO RECEIVING DATA #5
PC READING DATA #1
PC READING DATA #2
PC READING DATA #3
PC READING DATA #4
TIME PROGRESS
INDICATES SIO IS RECEIVING IDLE BYTES
INDICATES PC IS WAITING

Fig. 11

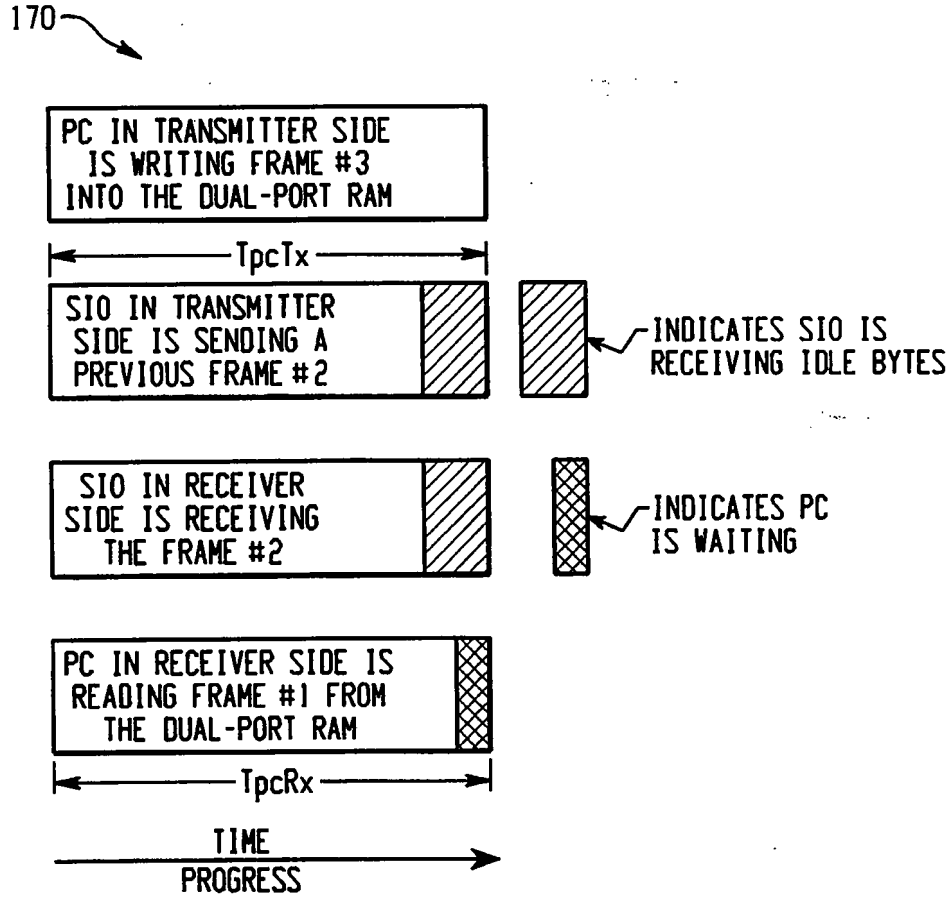

170
PC IN TRANSMITTER SIDE IS WRITING FRAME #3 INTO THE DUAL-PORT RAM
TpcTx
SIO IN TRANSMITTER SIDE IS SENDING A PREVIOUS FRAME #2
INDICATES SIO IS RECEIVING IDLE BYTES
SIO IN RECEIVER SIDE IS RECEIVING THE FRAME #2
INDICATES PC IS WAITING
PC IN RECEIVER SIDE IS READING FRAME #1 FROM THE DUAL-PORT RAM
TpcRx
TIME PROGRESS

Fig. 12

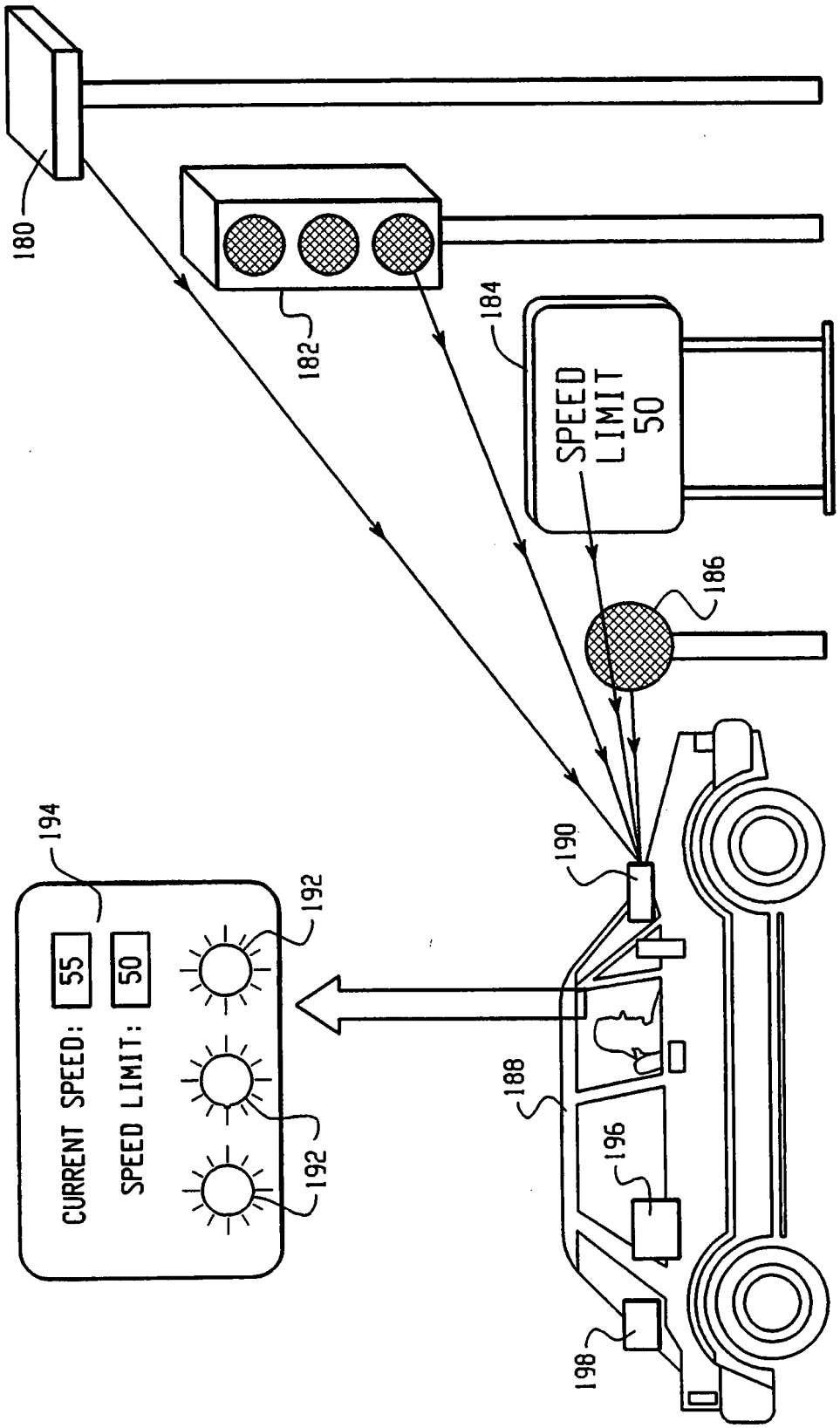

180
182
184
SPEED LIMIT 50
186
190
194
CURRENT SPEED: 55
SPEED LIMIT: 50
192
192
188
196
198

Fig. 13

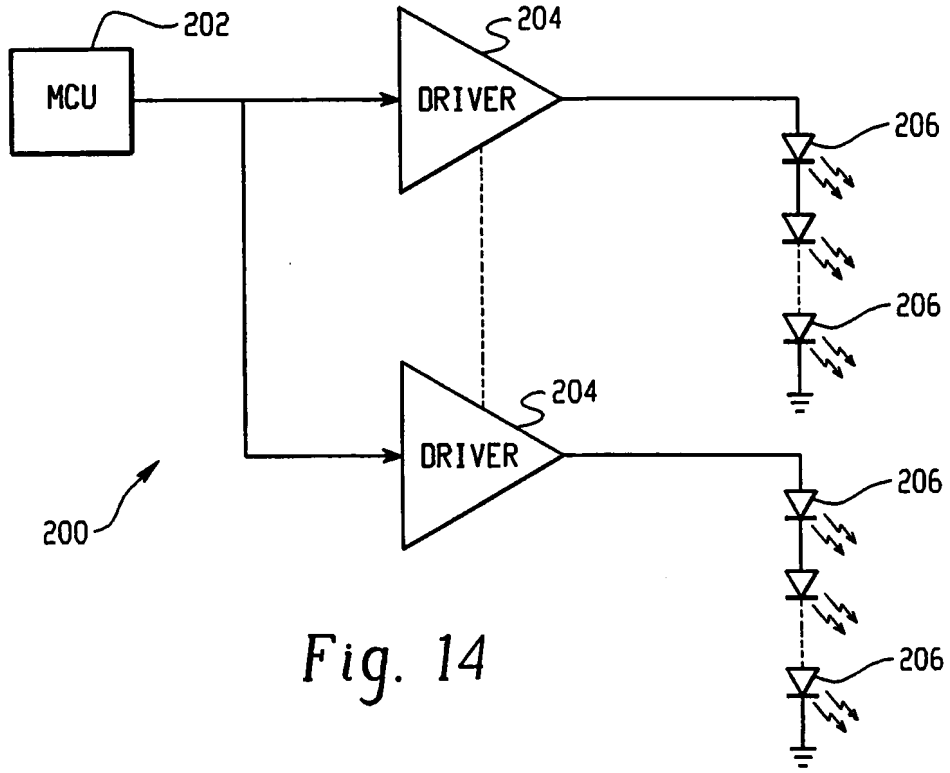


Fig. 14

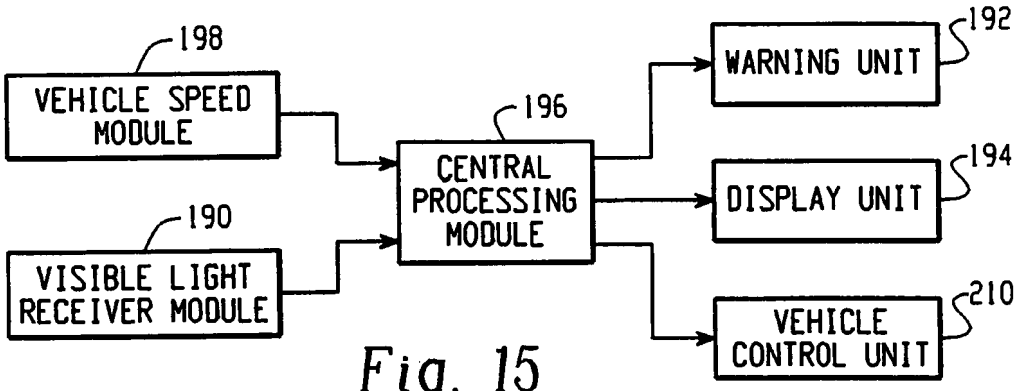


Fig. 15

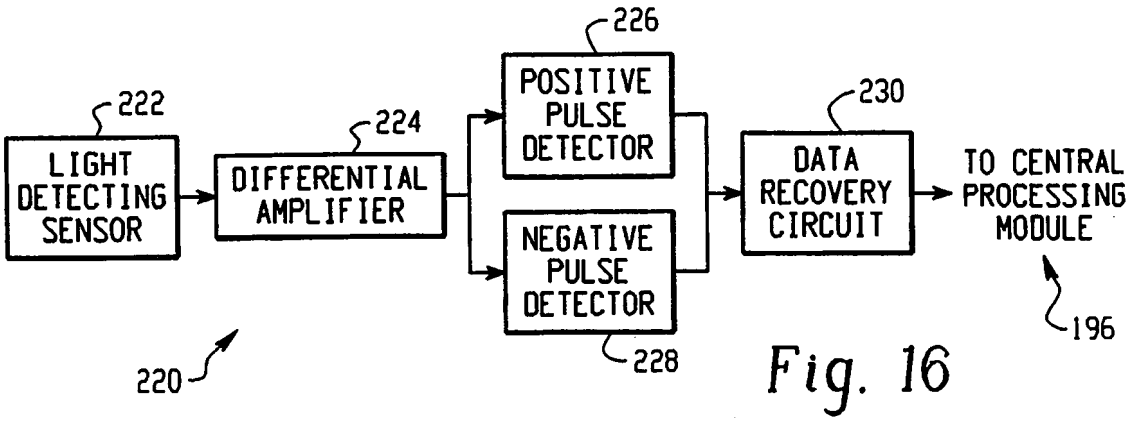
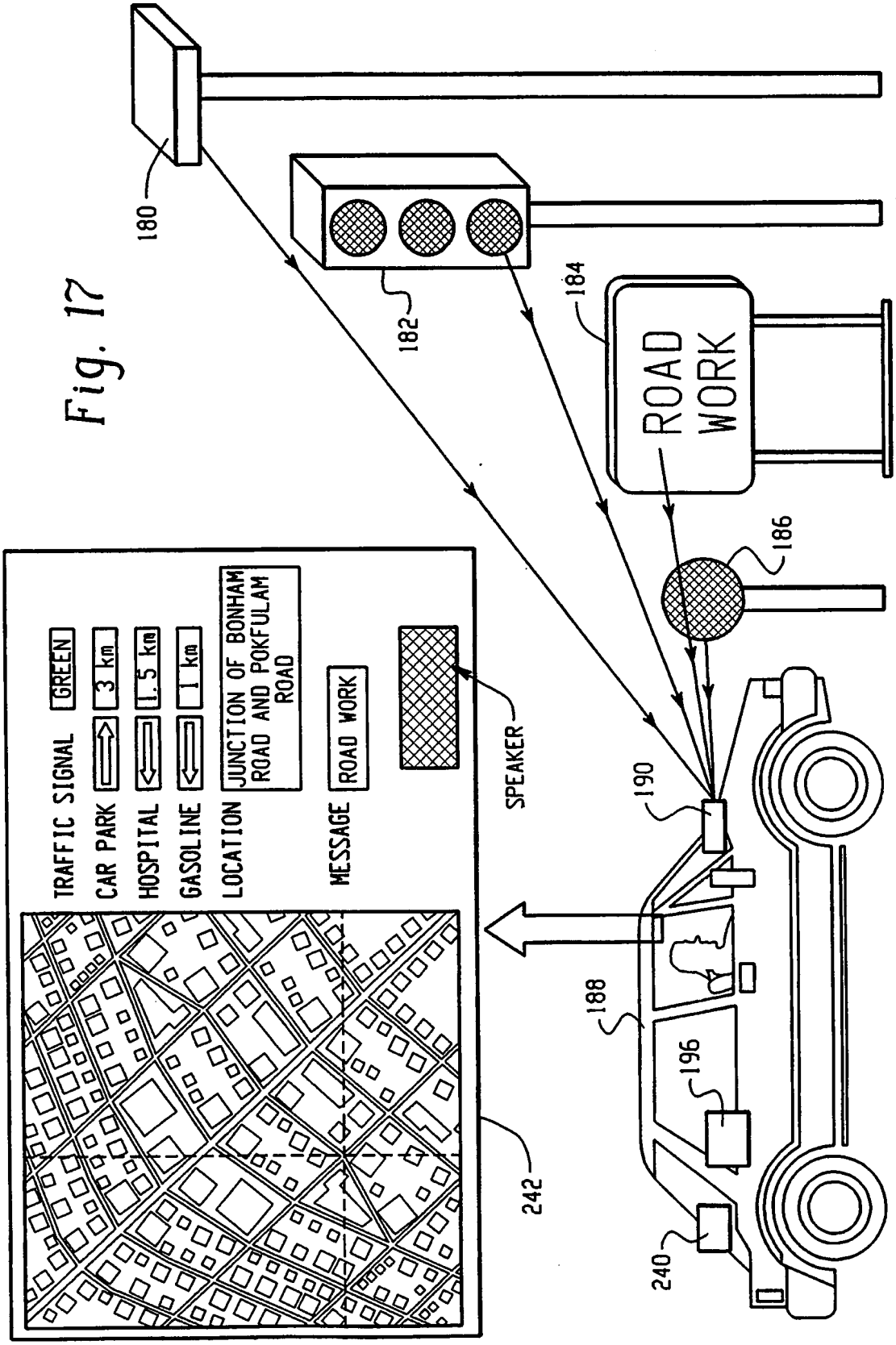


Fig. 16

Fig. 17


180
182
184
ROAD WORK
186
190
SPEAKER
TRAFFIC SIGNAL GREEN
CAR PARK 3 km
HOSPITAL 1.5 km
GASOLINE 1 km
LOCATION JUNCTION OF BONHAM ROAD AND POKFULAM ROAD
MESSAGE ROAD WORK
242
188
196
240

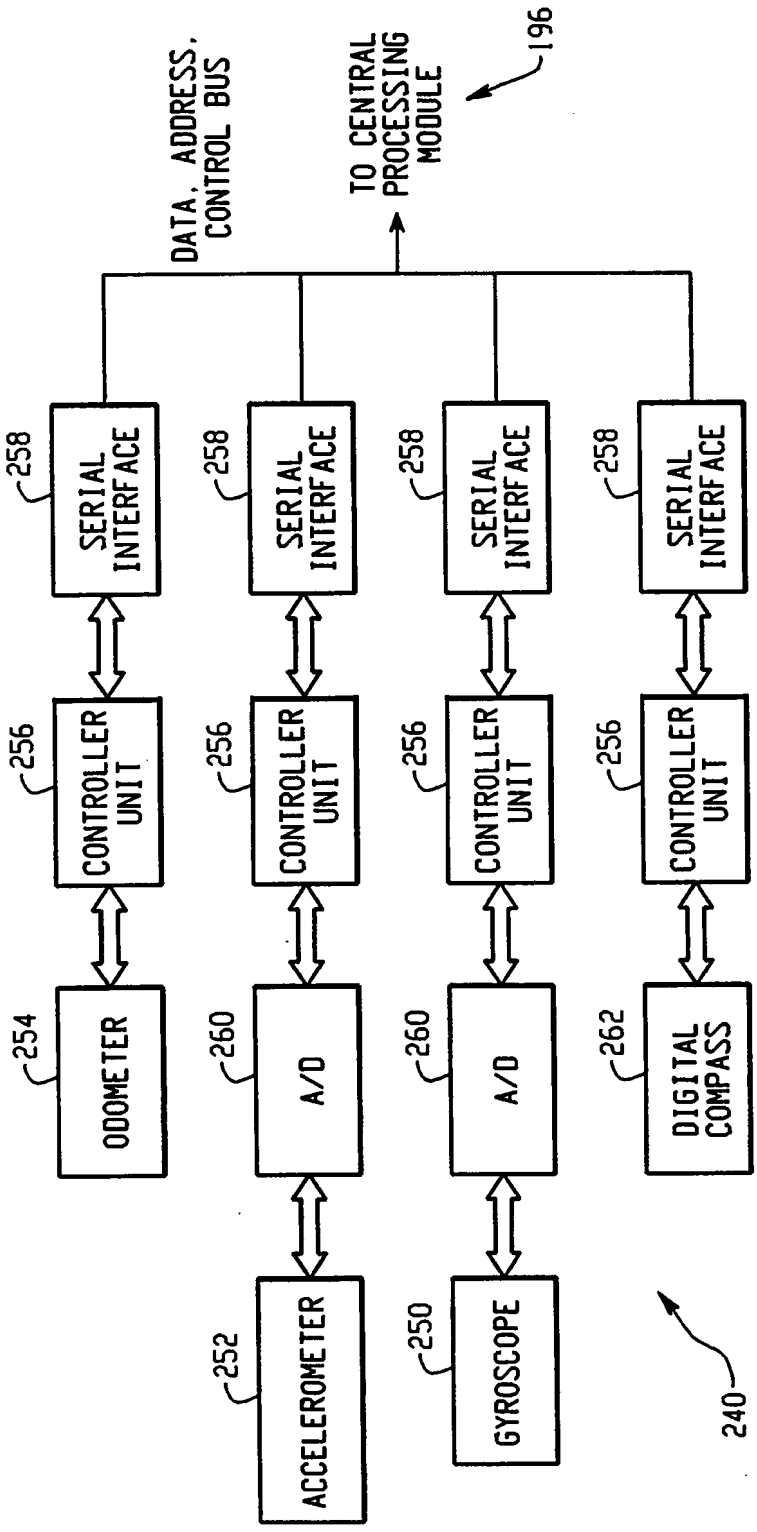

DATA, ADDRESS, CONTROL BUS
TO CENTRAL PROCESSING MODULE
196
SERIAL INTERFACE
258
CONTROLLER UNIT
256
ODOMETER
254
A/D
260
ACCELEROMETER
252
GYROSCOPE
250
DIGITAL COMPASS
262
240

Fig. 18

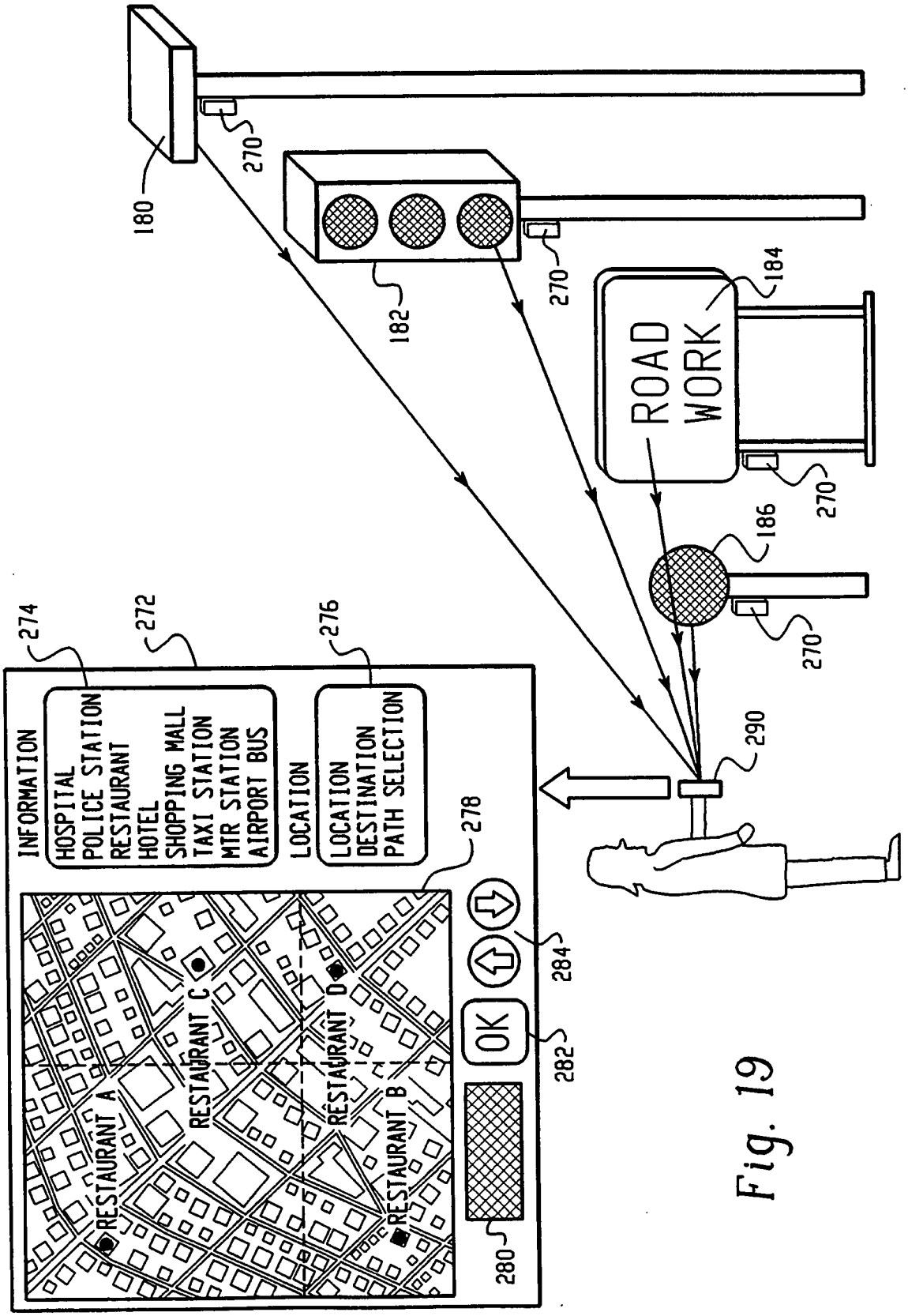

180
270
182
270
ROAD WORK
184
270
186
270
290
274
272
276
INFORMATION
HOSPITAL
POLICE STATION
RESTAURANT
HOTEL
SHOPPING MALL
TAXI STATION
MTR STATION
AIRPORT BUS
LOCATION
LOCATION
DESTINATION
PATH SELECTION
278
RESTAURANT A
RESTAURANT C
RESTAURANT D
RESTAURANT B
OK
284
282
280

Fig. 19

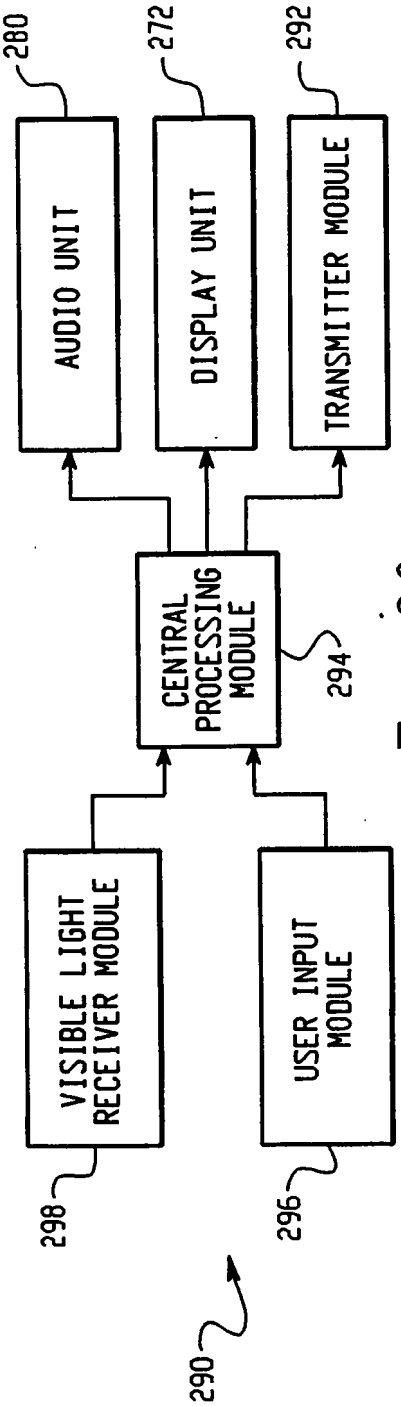

280
272
292
AUDIO UNIT
DISPLAY UNIT
TRANSMITTER MODULE
CENTRAL PROCESSING MODULE
294
VISIBLE LIGHT RECEIVER MODULE
USER INPUT MODULE
298
296
290

Fig. 20

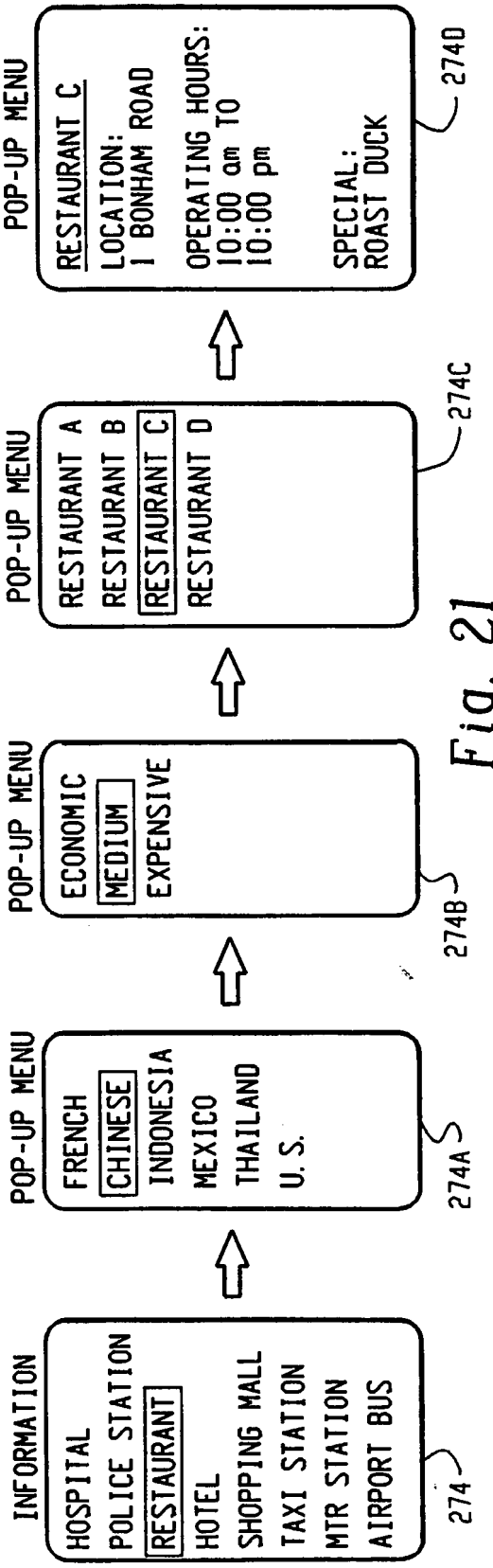

INFORMATION
HOSPITAL
POLICE STATION
RESTAURANT
HOTEL
SHOPPING MALL
TAXI STATION
MTR STATION
AIRPORT BUS
274
POP-UP MENU
FRENCH
CHINESE
INDONESIA
MEXICO
THAILAND
U.S.
274A
POP-UP MENU
ECONOMIC
MEDIUM
EXPENSIVE
274B
POP-UP MENU
RESTAURANT A
RESTAURANT B
RESTAURANT C
RESTAURANT D
274C
POP-UP MENU
RESTAURANT C
LOCATION:
1 BONHAM ROAD
OPERATING HOURS:
10:00 am TO
10:00 pm
SPECIAL:
ROAST DUCK
274D

Fig. 21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB99/00667

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) : GO8B 05/00; GO8G 01/09; GO8G 01/123
US CL : 340/815.4,905,995
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 340/815.4,905,995, 936,988,989,991,993,907; 701/117,210

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

None

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---- Y	US 5,633,629 A (HOCHSTEIN) 27 May 1997, Abstract; col.5, lines 15-37; col.6, lines 15-39; col.8, lines 62-67.	1-37,50-52,54-56,61-65,67,69 ---------- 38-49,53,57-60,66,68,70
Y,P	US 5,819,198 A (PERETZ) 06 October 1998, Abstract, col.3, lines 6-46.	38-49
Y	US 5,315,295 A (FUJII) 24 May 1994, Abstract.	47
Y	US 5,187,810 A (YONEYAMA et al.) 16 February 1993, Figure 5; col. 1, lines 23-42.	53,57-60, 66,68

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

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